UNITED STATES DISTRICT COURT
WESTERN DISTRICT OF TEXAS
WACO DIVISION

PARKERVISION, INC.,

Plaintiff,

v.

INTEL CORPORATION,

Defendant.

Case No. 6:20-cv-00562

JURY TRIAL DEMANDED

PLAINTIFF PARKERVISION'S
OPENING CLAIM CONSTRUCTION BRIEF

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I. Introduction.

The patents-in-suit relate to how wireless devices (e.g., cell phones) process radio signals. ParkerVision's constructions stay true to the intrinsic evidence. Intel, on the other hand, ignores the language of the specifications and *excludes* disclosed embodiments, improperly *injects limitations*, and applies Section 112 ¶ 6 for terms that do not include "means" language. Indeed, Intel seeks to *re-argue* positions, which this Court has already rejected in its January 28, 2021 Claim Construction Order in Case No. 6:20-cv-00108 (ECF No. 75). For the foregoing reasons, ParkerVision's constructions should be adopted and Intel's constructions should be rejected.

II. Intel seeks to *re-argue* terms this Court construed previously.

Term	Court's Prior Construction	Intel's Construction
"under-sample(s)"/ "under-sampling" ('706 patent, claims 1, 6, 7, 28, 34)	"sampling at less than or equal to twice the frequency of the input signal"	"samples at less than or equal to twice the frequency of the input signal using negligible apertures (i.e., pulse widths) that tend towards zero time in duration"
"storage module" ('706 patent, claims 105, 114, 164, 175, 179, 186, 190)	"a module of an energy transfer system that stores nonnegligible amounts of energy from an input electromagnetic signal"	"a module that stores a nonnegligible amount of energy from an input electromagnetic (EM) signal"
"switch" ('706 patent, claims 105, 164, 175, 186; '108 patent, claim 1)	Plain-and-ordinary meaning wherein the plain-and-ordinary meaning is "an electronic device for opening and closing a circuit as dictated by an independent control input"	"an electronic device for opening and closing a circuit"

The terms "under-sample(s)"/ "under-sampling," "storage module," and "switch" are in dispute in this case ("562 case"). The Court, however, has *already* construed these terms in related Case No. 6:20-cv-00108 ("108 case") and rejected Intel's constructions. *See* Ex. 1, Claim Construction Order dated January 28, 2021, *ParkerVision Inc. v. Intel Corp.*, No. 6:20-cv-00108, ECF No. 75. Intel seeks to *re-argue* these terms. But there are *no* new issues that Intel raises for

this Court to consider. Indeed, the parties have agreed to rely on their briefing from the 108 case for the terms "under-sample(s)"/ "under-sampling," "storage module," and "switch" in the 562 case. For the reasons set forth in ParkerVision's briefs in the 108 case, the Court in this case should adopt its prior constructions. *See ParkerVision Inc. v. Intel Corp.*, Case No. 6:20-cv-00108, ECF Nos. 51, 57, 65; *see also* Ex. 1.

III. Technology background.

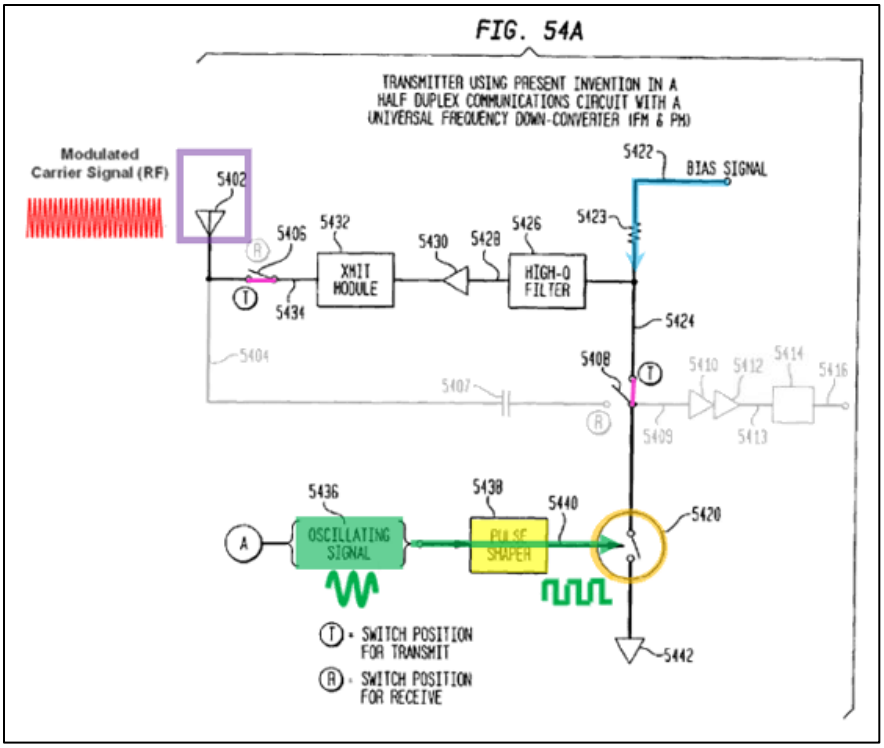
When two wireless devices (e.g., cellular phones) communicate, an RF signal (high-frequency signal) containing information (e.g., voice) (lower frequency signal) is sent from a transmitting device to a receiving device. At the transmitting device, the information is up-converted to an RF signal and sent over the air; at the receiving device, the RF signal is down-converted to recover the information carried on the RF signal. A discussion of wireless technology is set forth in ParkerVision's Opening Claim Construction Brief in the 108 case. *See* Plaintiff ParkerVision's Opening Claim Construction Brief, *ParkerVision Inc. v. Intel Corp.*, No. 6:20-cv-00108, ECF No. 51 at Sections II-III.

IV. The patents-in-suit.

A. The patents-in-suit pertain to up-conversion and down-conversion of RF signals. Transmitter/up-conversion – U.S. Patent Nos. 7,050,508 and 8,190,108

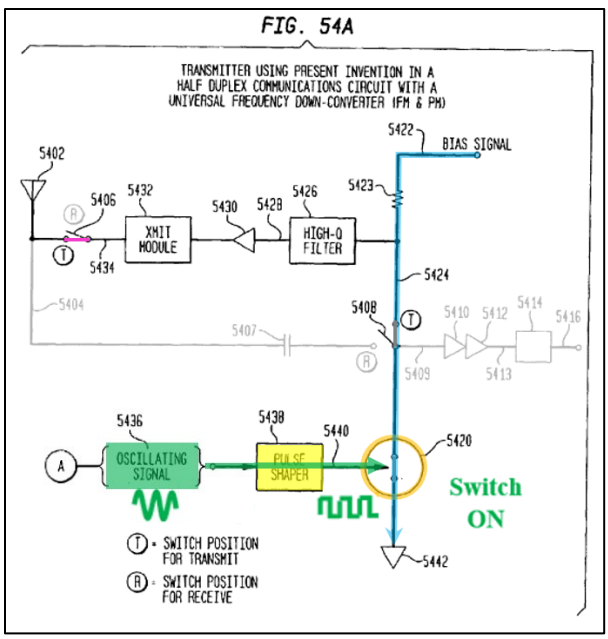
Figure 54A of the '508 patent (below) illustrates components of an exemplary up-conversion system, which would be incorporated into a transceiver chip of a wireless device.[1] The up-conversion system includes a switch 5420 (orange), a control signal (green), a bias signal 5422 (blue) and an antenna 5402 (purple).

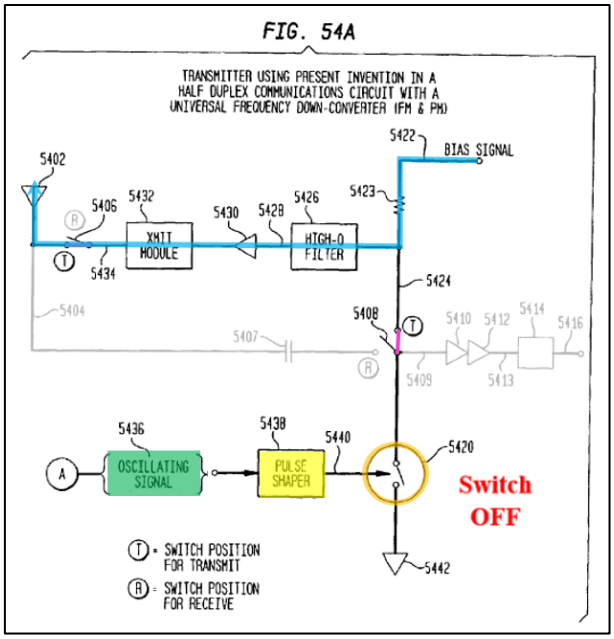
[1] Figure 54A illustrates components of both up-conversion (transmission) and down-conversion (reception) systems. The down-conversion (reception) system components are grayed out as they are not relevant to a discussion of the up-conversion (transmission) system.

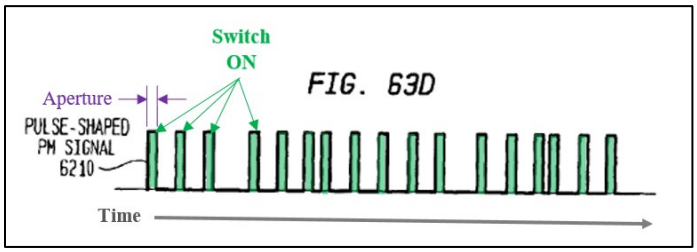


As shown above, in the transmit mode, the switches 5406 and 5408 are positioned as shown by the pink lines.[2] An oscillator (not shown) generates an oscillating (sinusoidal) signal 5436 (green sinusoidal wave form), which is transmitted to and shaped by the pulse shaper 5438 (yellow) into a string of pulses 5440 (green square wave form). The string of pulses 5440 controls the opening and closing of the switch 5420 (orange).

[2] Figure 54A uses the symbol Ⓣ to represent the switch position for signal transmission and the symbol Ⓡ to represent the switch position for signal reception. The switches are positioned towards the Ⓣ during transmission and towards the Ⓡ during reception.







The annotations in Figure 54A above illustrate how information (baseband/low frequency signals) is up-converted to a high frequency RF signal (modulated carrier signal). In particular, up-conversion occurs by repetitively turning the switch 5420 ON (closed) and OFF (opened).

As shown in Figure 63D above, the switch is turned ON (closed) by sending a pulse (green) to the switch. The switch is kept ON (kept closed) for the duration of the pulse (i.e., during a *non*-negligible aperture (purple) of the pulse). As shown by the repetitive string of pulses, this opening/closing of the switch continues over time.

As shown in Figure 54A (above left), when the switch is ON (closed) during the aperture, the bias signal 5422 (blue) passes to ground 5442. As shown in Figure 54A (above right), when the energy pulse stops, the switch is turned OFF (opened) and the bias signal 5422 (blue) is sent

to the antenna 5402.

FIG. 63E

FIG. 63F

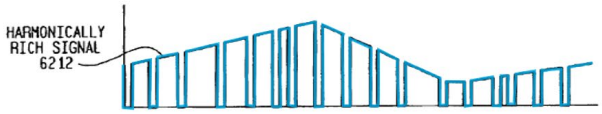


Figure 63E above (left) illustrates an exemplary reference (bias) signal 6206. As shown in Figure 63F above (right), repetitively turning the switch ON (closed) and OFF (open) affects the shape of reference (bias) signal 6206, resulting in a square wave signal 6212. The valleys in the signal 6212 are created when the switch is turned ON (closed) and portions of the reference (bias) signal passes to ground 5422. The peaks in the signal 6212 are created when the switch is turned OFF (opened).

FIG. 63G

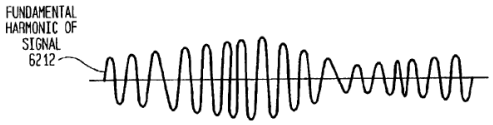
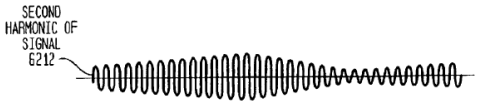
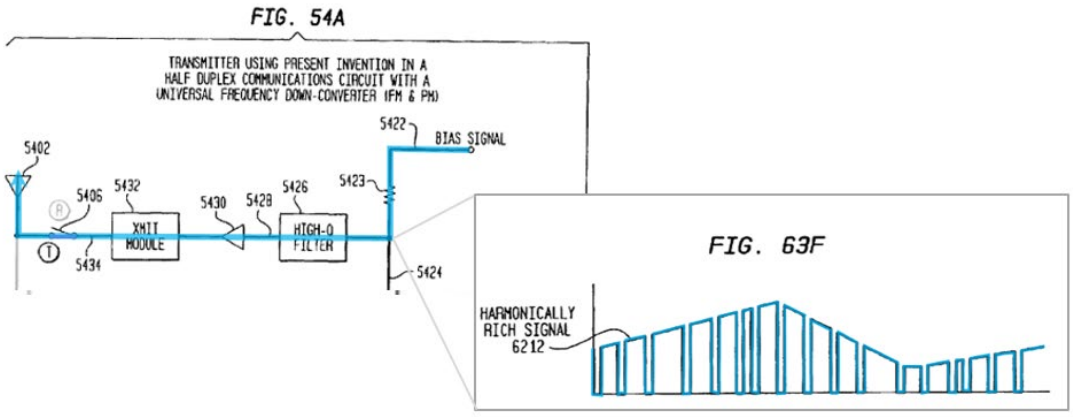


FIG. 63H



The signal 6212 (Figure 63F) is referred to as a harmonically rich signal because the signal 6212 is actually made up of numerous sinusodial signals (harmonics) such as those signals shown above in Figures 63G and 63H. The combination of sinusodial signals (harmonics) form the signal 6212.



As shown above, the harmonically rich signal 6212 (Figure 63F) passes through a filter 5426 on its ways to the antenna 5402. The filter 5426 filters out certain harmonics so that only a subset of all harmonics are transmitted from the antenna 5402. This filtering produces a clean signal that can carry the information over the air.

B. Receiver/down-conversion– U.S. Patent No. 6,049,706

The '706 patent pertains to how a receiving wireless device down-converts an RF signal. Down-conversion is described in Plaintiff ParkerVision's Opening Claim Construction Brief in Case No. 6:20-cv-00108 (ECF No. 51), which is briefly summarized below.

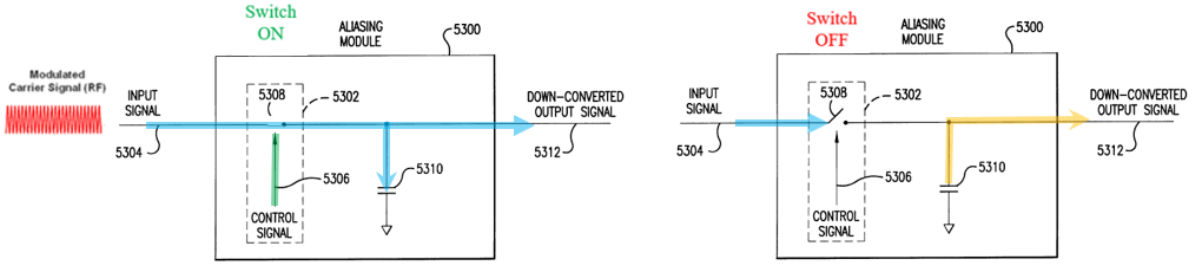


FIG. 53A FIG. 53A

The figures above illustrate components of the receiving device that are used to extract information (e.g., voice) from the received RF signal. In order to obtain and process the information that was sent from the transmitting device, the receiving device must down-convert

the RF signal to a lower frequency signal. As shown above, the system uses a switch 5308, capacitor 5310, and control signal 5306 having pulses with *non*-negligible apertures. '706 patent, 32:9-18. The control signal 5306 (green) turns the switch ON (closed) and OFF (open). As shown by the blue line, when the switch 5308 is ON (closed), energy (1) flows to the capacitor 5310 and a low impedance load (not shown), and (2) is stored in the capacitor 5310. As shown by the orange line, when the switch is OFF (open), energy stored in capacitor 5310 flows to a low impedance load.

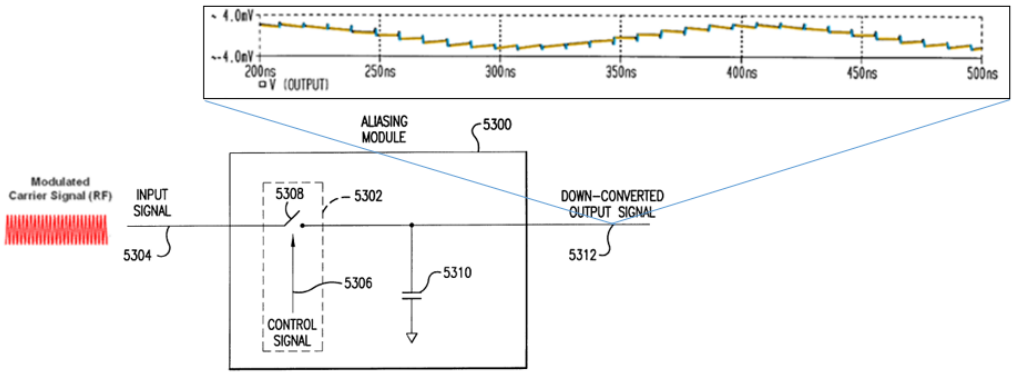


FIG. 53A

As shown above, turning the switch ON and OFF results in the creation of the blue/orange waveform, which is the down-converted signal 5312 contained within the RF signal.

V. U.S. Patent No. 6,049,706 – Disputed terms for construction

A. "down-convert and delay module" (claims 1, 7)

ParkerVision's Construction	Intel's Construction
Not subject to 35 U.S.C. § 112, ¶ 6 Plain and ordinary meaning	Subject to 35 U.S.C. § 112, ¶ 6 Function: under-sample an input signal to produce an input sample of a down-converted image of said input signal, and to delay said input sample Structure: the down convert and delay module 2624 in Fig. 26 and described at 26:1-27:21

	and 28:20-41, that includes the switches 2650 and 2654, the scalers 2690A and 2690B, and the capacitors 2652 and 2656; and equivalents thereof

The term is straight-forward and does not require a construction. Despite the structural nature of "*down-convert and delay* module," Intel asserts that the term implicates 35 U.S.C. §112, ¶ 6. Intel is incorrect. *First*, the term does *not* use the word "means." Thus, there is a presumption that §112, ¶ 6 does *not* apply. *Williamson v. Citrix Online, LLC,* 792 F.3d 1339, 1348 (Fed. Cir. 2015) (en banc) (noting that "failure to use the word 'means' also created a rebuttable presumption—this time that former § 112, para. 6 does not apply."). *Second*, the claims recite a definite structure. Indeed, the claims do not simply recite a "module," but recite a specific type of module – "*down-convert and delay* module." A "*down-convert and delay* module" has a known structure that incorporates components/circuits such as a switch (the opening and closing of which down-converts a signal) and a capacitor/storage element (for storing/delaying a signal).[3] *See, e.g.,* '706 patent, 28:24-25.

Indeed, dependent claims 3 and 4 make it clear that the "*down-convert and delay* module" includes such structural components/circuits. And the dependent claims must be considered in determining the applicability of § 112, ¶ 6. *See, e.g., TEK Global, S.R.L. v. Sealant Sys. Int'l, Inc.*, 920 F.3d 777, 786 (Fed. Cir. 2019) ("[T]he dependent claims suggest that § 112, ¶ 6 does not govern. Indeed, they 'add limitations that either describe particular structural features or flesh out whether the term has a particular structural meaning.'"). In particular, dependent claim 3 not only discloses the structural components/circuits of the "*down-convert*

[3] Notably, Intel's own construction identifies the structure as switches and capacitors.

and delay module" – switch, storage element (e.g., capacitor), nodes and reference potential (e.g., ground) – but also describes their *physical* connections: "a *switch* and a *storage element*, wherein a first *node* of said *storage element* is coupled to a *node* of said *switch*, and a second *node* of said *storage element* is coupled to a *reference potential*." '706 patent, 45:39-43. Claim 4 includes similar structural components. *Id*. at 45:44-48. Thus, the presumption *against* §112, ¶ 6 stands. *See TEK Global*, 920 F.3d at 786.

For the foregoing reasons, the term is *not* subject to §112, ¶ 6[4] and it should be given its plain and ordinary meaning.

B. "said input sample", "said sample" (claims 1, 6, 7, 34)

ParkerVision's Construction	Intel's Construction
Plain and ordinary meaning	"the sample of the image that has been down-converted"

The claim language is straightforward and no construction is necessary. The terms "said input sample" and "said sample" simply refer back to their respective antecedent bases. Claims 1 and 7,[5] for example, recite "a down-convert and delay module to under-sample an input signal to

[4] Even if §112, ¶ 6 applies (which it doesn't), Intel's construction is wrong. *First*, Intel's construction is missing one of the functions of the "down-convert and delay module" set forth in the claims – "under-sampl[ing] said input signal according to a control signal." *See* '706 patent, 45:29-30. *Second*, Intel's construction is missing relevant structures of the "down-convert and delay module." Intel seeks to *limit* the structure to an embodiment of a system that under-samples using negligible apertures (Figure 26) while *excluding* an embodiment that under-samples using *non*-negligible apertures (Figures 53A, 53A-1). Intel's reasons for excluding the *non*-negligible apertures embodiment is its view that "under-sampling" is performed only using negligible apertures. But after briefing and oral arguments at the hearing, this Court has already rejected Intel's position in the 108 case. The Court declined to limit the construction of "under-sampling" to sampling using negligible apertures in the Court's January 28, 2021 Claim Construction Order. *See* Ex. 1 at 3. As such, Intel's construction of the structure is missing the switches and capacitors in Figures 53A and 53A-1. *Finally*, Intel's structure is missing the "down-convert and delay module" 1708, 1908, 2308 of Figures 17, 19 and 23, respectively, which are described, e.g., in Section 3.4.2.1. *See* '706 patent 27:65-32:25.

[5] Claim 6 of the '706 patent uses similar language: "(a) means for under-sampling an input signal to produce *an input sample of a down-converted image of said input signal* and (b) first delaying

produce *an input sample of a down-converted image of said input signal*, and to delay *said input sample*." '706 patent, 45:15-18; 46:9-12. As such, "said input sample" simply refers back to the "input sample of a down-converted image of said input signal." Similarly, claim 34 recites "a frequency translator to produce *a sample of a down-converted image of an input signal*, and to delay *said sample*." *Id.* at 48:46-48. As such, "said input sample" simply refers back to the "sample of a down-converted image of an input signal."

As written, the claims require a relationship between the sample and the input signal – the sample is taken from the input signal. But Intel seeks to negate this claimed relationship. Intel attempts to *change* the meaning of the claims to remove this relationship so that the sample that is delayed is no longer tied to the input signal.

With regard to claims 1, 6 and 7, not only does Intel inexplicably *re-arrange* the claim language as written[6] – changing "sample of a down-converted image" to "sample of the image that has been down-converted" – and *change* "input sample" to "sample," but Intel *omits* the critical language "of said input signal." Similarly, with regard to claim 34, Intel re-arranges the claim language as written and omits the language "of an input signal." By removing "of [said/an] input sample" in all of the claims, Intel seeks to sever the relationship between the sample and the input signal.

For the foregoing reasons, Intel's attempt to *re-write* the claim language should be rejected and the term should be given its plain and ordinary meaning.

C. "delay module" (claims 1, 7, 34, 140)

ParkerVision's Construction	Intel's Construction
Not subject to 35 U.S.C. § 112, ¶ 6	Subject to 35 U.S.C. § 112, ¶ 6

means for delaying *said input sample*." '706 patent, 45:54-56. As such, the same arguments apply.

[6] By re-arranging the claim language, Intel hopes to obfuscate its re-write of the claims.

Plain and ordinary meaning	Function: delay instances of an output signal / further delay one or more of said delayed and down-converted input samples Structure: structure including "first delay module 2628," "second delay module 2630" shown in Fig 26, "delay module 3204" shown in Fig. 32 and described at 35:1-18; the sample and hold circuit 4501 and 4503 in Fig. 45 and described at 32:44-33:19; or an analog delay line having a combination of capacitors, inductors and/or resistors described at 35:19-27; or equivalents thereof that operate to delay samples/instances of a signal presented at its input by a known amount.

The term is straight-forward and does not require a construction. Despite the structural nature of "*delay* module," Intel asserts that the term implicates 35 U.S.C. §112, ¶ 6. Similar to its position on the "down-convert and delay module," Intel is incorrect. Once again, the term does *not* use the word "means." Thus, there is a presumption that §112, ¶ 6 does *not* apply. *Williamson,* 792 F.3d at 1348. And the claims recite a definite structure. Indeed, the claims do not simply recite a "module," but recite a specific type of module – "*delay* module." A "*delay* module" has a known structure that incorporates components/ circuits, such as a capacitor (for storing/delaying a signal).[7] *See e.g.*, '706 patent, Figures 17, 19, 23, 32, 34; 34:60-35:31.

For the foregoing reasons, the term is *not* subject to §112, ¶ 6[8] and it should be given its plain and ordinary meaning.

[7] Notably, Intel's own construction identifies the structure as including capacitors.
[8] Even if §112, ¶ 6 applies (which it doesn't), Intel's construction is wrong. Intel's structure is missing the "delay modules" 1722A, 1722B, 1722C in Figure 17, "delay modules" 1912, 1914 in Figure 19, and "delay modules" 2316, 2318 in Figure 23, which are described, e.g., in Section 3.4.2.2. *See, e.g.,* '706 patent, Figures 32, 34; 34:60-35:31.

D. "harmonic" / "harmonics" ('706 patent, claims 1, 6, 7, 28, 34; '508 patent, claim 1)

Patent No.	ParkerVision's Construction	Intel's Construction
"harmonic" ('706 patent, claims 1, 6, 7, 28, 34)	"A sinusoidal component of a periodic wave that has a frequency that is an integer multiple of the fundamental frequency of the periodic waveform and including the fundamental frequency as the first harmonic"	"A sinusoidal component of a periodic wave that has a frequency that is an integer multiple of the fundamental frequency of the periodic wave"
"harmonic(s)" ('508 patent, claim 1)	"a frequency or tone that, when compared to its fundamental or reference frequency or tone, is an integer multiple of the fundamental frequency of the periodic waveform and including the fundamental frequency as the first harmonic"	"Sinusoidal components of a periodic wave each of which have a frequency that is an integer multiple of the fundamental frequency of the periodic wave"

Since the '706 and '508 patents both include the term "harmonic(s)," ParkerVision will address these patents together.

Though the parties use different language, *with one key exception*, the parties' constructions are fundamentally the same. At bottom, the parties' dispute is whether the "fundamental frequency" of a periodic waveform is a "harmonic." Consistent with ParkerVision's construction, the *lexicography* in the specifications demonstrate that the "fundamental frequency" is a "harmonic."[9] Indeed, the "fundamental frequency" is referred to in the specification as "the *first harmonic*." And, as discussed below, another district court (that construed ParkerVision's patents) held that the fundamental frequency is a harmonic. Thus, ParkerVision's construction includes the fundamental frequency as one of the frequencies of a

[9] It is notable that in litigation ParkerVision brought against Qualcomm in the U.S. District Court for the Middle District of Florida (Orlando) involving the same patent disclosure, Qualcomm, a highly sophisticated party and the industry leader in wireless chip technology, *agreed* to the construction ParkerVision proposes in this case. Ex. 2, Order dated Apr. 29, 2020 at 10.

periodic waveform i.e., one of the harmonics.

On the other hand, Intel's construction purposefully remains silent regarding the fundamental frequency, hoping to avoid raising a red flag to the Court at this time and preserve a non-infringement argument. Intel omits reference to the "fundamental frequency" because, as Intel stated during the parties' meet-and-confer, Intel's position is that the "fundamental frequency" is *not* one of the harmonics of a periodic wave. In other words, Intel seeks to *exclude* the fundamental frequency as being a harmonic. But, as set forth below, Intel is wrong.

Wireless devices include wireless chips. These chips are responsible for transmitting information (e.g., voice and data) over the air. In order to transmit the information, the transmission components of the chip create a signal (a continuous periodic waveform) that carries the information. This continuous periodic waveform, in turn, is made up of a number of sinusoidal signals referred to as harmonics. *See* Section IV.A above.

Notably, *every* waveform has a *first harmonic* (fundamental frequency) as well as *additional* harmonics (second harmonic, third harmonic, and so on) whose frequencies are a function of the first harmonic (fundamental frequency). As such, the fundamental frequency being the first harmonic is not merely an embodiment; the fundamental frequency is *always* a harmonic.

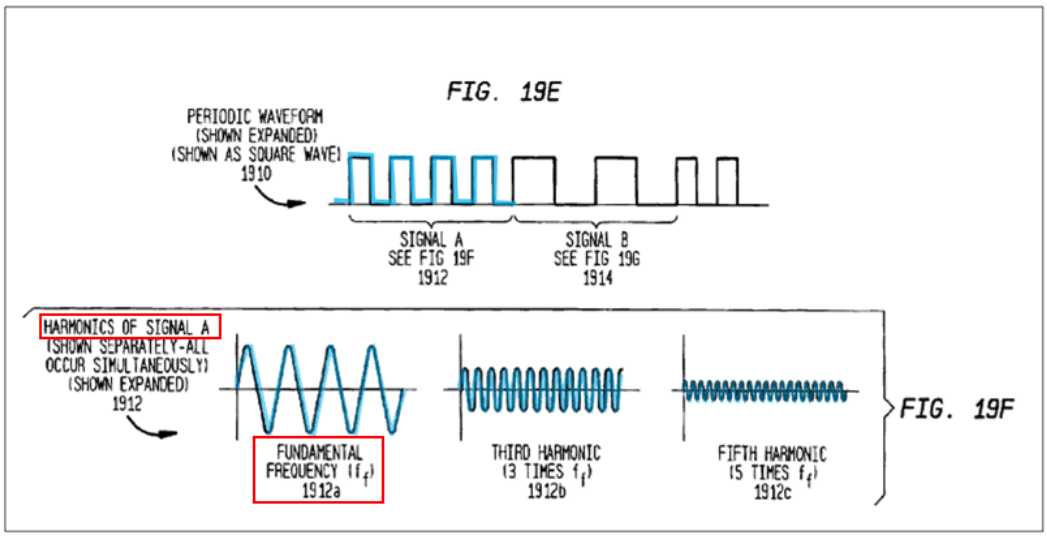


Figure 19E of the '508 patent, above, illustrates a periodic waveform 1912 (blue) that is generated by a wireless device. Figure 19F shows the *first harmonic* (fundamental frequency f_f), the third harmonic, and the fifth harmonic.[10] *See also* Figure 19G (showing the fundamental frequency f_f as the first harmonic). Notably, the fundamental frequency is a harmonic.

The '508 patent and '706 patent are directed to different technologies[11] and each patent has its own lexicography regarding the meaning of "harmonic." Intel's constructions ignore this difference.[12] Nevertheless, in both cases, the lexicography demonstrates that the fundamental frequency is a harmonic. *C.R. Bard, Inc. v. U.S. Surgical Corp.*, 388 F.3d 858, 862 (Fed. Cir. 2004) ("[T]he inventor's written description of the invention, for example, is relevant and controlling insofar as it provides clear lexicography ….").

[10] As shown above, the third and fifth harmonics are functions of the fundamental frequency f_f. The third harmonic has a frequency that is three times the fundamental frequency f_f (i.e., 3 x f_f); the fifth harmonic has a frequency that is five times the fundamental frequency f_f (i.e., 5 x f_f).
[11] The '508 patent is directed to how a signal is up-converted for transmission from a wireless device, whereas the '706 patent is directed to how a signal is down-converted after being received by a wireless device.
[12] Intel's construction for the '508 patent ignores the lexicography and, instead, improperly uses the lexicography from the '706 patent.

The '706 patent provides the following lexicography:

> Harmonic: *A harmonic is a sinusoidal component of a periodic wave. It has a frequency that is an integer multiple of the fundamental frequency of the periodic wave.* In other words, if the periodic waveform has a *fundamental frequency of "f" (also called the first harmonic)*, then it has harmonics at frequencies of 'n•f,' where 'n' is 2, 3, 4, etc. The harmonic corresponding to n=2 is referred to as the second harmonic, the harmonic corresponding to n=3 is referred to as the third harmonic, and so on.

'706 patent, 9:39-47.

The '508 patent provides the following lexicography:

> Harmonic: *A harmonic is a frequency or tone that, when compared to its fundamental or reference frequency or tone, is an integer multiple of it.* In other words, if a periodic waveform has a *fundamental frequency of 'f' (also called the first harmonic)*,[13] then its harmonics may be located at frequencies of 'n•f,' where 'n' is 2, 3, 4, etc. The harmonic corresponding to n=2 is referred to as the second harmonic, the harmonic corresponding to n=3 is referred to as the third harmonic, and so on.

'508 patent, 9:53-61.

Indeed, the fact that the fundamental frequency is a harmonic ("the first harmonic") (i.e., that the first harmonic is one the claimed harmonics) is discussed throughout the specifications.

> As shown in FIG. 19, if rectangular waveform 1908 has a *fundamental frequency of f_1 (also known as the first harmonic)*, the third harmonic will have a frequency of 3 • f_1, the fifth harmonic will have a frequency of 5 • f_1, and so on.

Id. at 20:11-15.

> The most basic waveform which is continuous and periodic is a sine wave. It has but *one harmonic, which is at the fundamental frequency*. This is *also called the first harmonic*."

Id. at 43:16-19; *see also id.* at 22:60-66 ("In step 1314, a filter 1414 filters out the undesired *harmonic frequencies* (for example, the *first harmonic* 4410, the second harmonic 4412, and the

[13] All periodic waveforms have a fundamental frequency (first harmonic). As such, this language is merely expressing the formula for determining the other harmonics of the waveform assuming that the fundamental frequency is denoted by "f."

fourth, fifth, etc., harmonics, not shown), and outputs an electromagnetic (EM) signal 1416 at the desired harmonic frequency . . . ."); *id.* at 43:47-50 ("Thus, if the frequency of the rectangular waveform is F_r, then the *frequency of the first harmonic is 1• F_r*, the frequency of the second harmonic is 2•F_r, the frequency of the third harmonic is 3• F_r, and so on.") *id.* at 24:62-65.

The fundamental frequency is the first harmonic because the specification discloses that "there are harmonics at *all of the multiples* of the fundamental frequency." *Id.* at 43:45-47. Indeed, the numbers (n) *1*, 2, 3, 4, etc. are all integers (whole numbers) and, thus, are all integer multiples. The formula for determining the frequency of the harmonics is: frequency = n x F_r, where "n" is an integer multiple. In particular, the specification discloses that the first harmonic is at a frequency that is 1 times (i.e., n=1) the fundamental frequency F_r. Since 1 x F_r = F_r, the first harmonic is at the frequency of the fundamental frequency.

> A more typical waveform is a rectangular wave, which is a series of pulses. Each pulse will have a width . . . and the series of pulses in the waveform will have a period ('T' which is the inverse of the frequency, i.e., T=1/F_r, where *'F_r' is the fundamental frequency of the rectangular wave*). . . . *The mathematical analysis shows that there are harmonics at all of the multiples of the fundamental frequency of the signal*. Thus, if the frequency of the rectangular waveform is F_r, then the *frequency of the first harmonic is 1• F_r*, the frequency of the second harmonic is 2•F_r, the frequency of the third harmonic is 3• F_r, and so on.

See id. at 43:33-50. The specifications disclose other instances where n=1. *See, e.g., id.* at 63:30-31; '706 patent, 30:22-24 ("The value of n represents a harmonic or sub-harmonic of input signal [] (e.g., n = 0.5, *1*, 2, 3, …).."). In other words, 1 is an integer multiple.

Though the Court will make its own determination regarding the meaning of "harmonic," there is prior litigation history related to this term that ParkerVision would like to bring to the Court's attention. ParkerVision's constructions of "harmonic(s)" adopt the view of the U.S. District Court for the Middle District of Florida (Jacksonville) (Case No. 3:11-cv-00719). Ex. 3, Order dated Feb. 20, 2013 at 16-17. In reaching its conclusion related to "harmonic," the

Jacksonville court concluded that the fundamental frequency is a harmonic (i.e., n=1). *Id.* at 17.

Intel seeks to ignore the lexicography, the specifications' disclosures regarding the fundamental frequency being a harmonic, and the Jacksonville court's ruling. Intel's position is that the integer 1 (n=1) is not an "integer multiple" and, thus, the fundamental frequency (n=1) is not a harmonic. As set forth above, Intel is incorrect. Though the specifications certainly state that integers 2, 3, 4, etc. (n=2, 3, 4, etc.) are "integer multiples," as set forth above, the specifications also make it clear that the integer 1 (n=1) is an integer multiple. Indeed, there is nothing in the specifications that excludes the integer 1 (n=1) from being an "integer multiple." As such, the fundamental frequency is a harmonic, which is consistent with the express disclosures that the fundamental frequency is "the first harmonic."

For the foregoing reasons, Intel's gamesmanship should be rejected, and ParkerVision's construction should be adopted.

E. "pulse widths that are established to improve energy transfer" (claim 2)

ParkerVision's Construction	**Intel's Construction**
Plain and ordinary meaning pulse widths that use non-negligible apertures for energy transfer	Indefinite

Contrary to Intel's position, the term is *not* indefinite. Claim 1 of the '706 patent recites a "down-convert and delay module under-samples said input signal according to a control signal." Claim 2, which depends from claim 1, recites that the "control signal comprises a train of pulses having *pulse widths that are established to improve energy transfer* from said input signal to said down-converted image."

The language "*pulse widths that are established to improve energy transfer*" simply means that pulses having *non*-negligible apertures are being used. Pulses having *non*-negligible

apertures "improve" energy transfer. In particular, as discussed below, the specification informs a skilled person to use pulses with *non*-negligible apertures (which tend away from zero) in order to "improve" energy transfer instead of pulses that have negligible apertures (which tend towards zero). By using *non*-negligible apertures, more energy is transferred to a storage device (capacitor) from an input signal than would be transferred by using negligible apertures – hence the language "improve energy transfer."

As shown, for example, in Figure 53A of the '706 patent below, an aliasing module 5300 (down-convert and delay module) (purple) receives an input signal 5304. The module 5300 includes a switch 5308 (blue) and capacitor 5310 (orange).

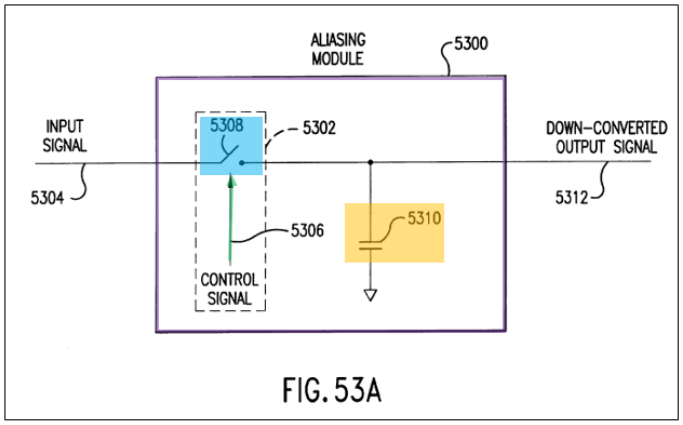


FIG. 53A

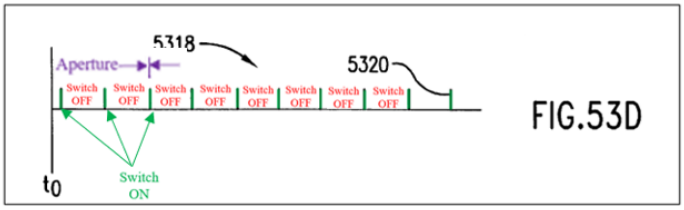


FIG.53D

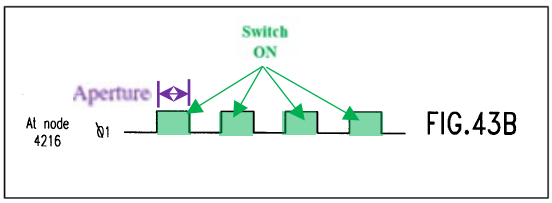
Figure 53D, above, illustrates a control signal 5306 having a train of pulses 5320 (green) "having *negligible* apertures that tend towards zero." '706 patent, 29:31-41. The switch 5308 is turned ON (closed) for the time period during which the switch receives a control signal 5306 (green) (during the duration of the aperture (purple)). When the switch is turned ON (closed),

energy from the input signal 5304 is transferred to the capacitor 5310. When the control signal stops, the switch is turned OFF (opened) and energy from the input signal 5304 is no longer transferred to the capacitor 5310. Since the aperture (purple) is *very short*, only a *negligible* amount of energy is transferred to the capacitor 5310.

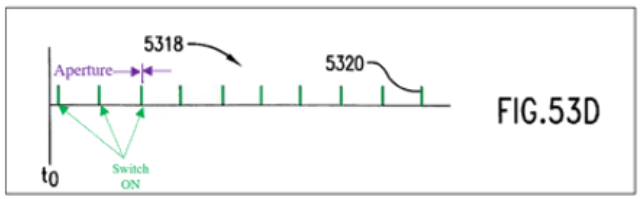
Importantly, the specification provides guidance to a skilled person as to how to improve energy transfer. *See Interval Licensing LLC v. AOL, Inc.*, 766 F.3d 1364, 1370 (Fed. Cir. 2014) ("Claim language employing terms of degree has long been found definite where it provided enough certainty to one of skill in the art when read in the context of the invention."). In particular, the specification states that energy transferred is "improved" by using "*non*-negligible apertures" instead of negligible apertures.

> In another embodiment, the pulses of the control signal 5306 have *non-negligible apertures that tend away from zero*. This makes the UFT module 5302 a lower input impedance device. This allows the lower input impedance of the UFT module 5302 to be substantially matched with a source impedance of the input signal 5304. This also *improves the energy transfer from the input signal 5304 to the down-converted output signal 5312*, and hence the efficiency and signal to noise (sin) ratio of UFT module 5302.

'706 patent, 32:9-18.



***Non*-negligible apertures**



Negligible apertures

As shown in Figure 43B (above left), the pulses (green) with *non*-negligible apertures (purple) have widths that are *greater than* the pulses (green) with negligible apertures (purple) of Figure 53D (above right). Because pulses with *non*-negigible apertures have a *greater width* than pulses with negligible apertures, the switch 5308 is ON (closed) *longer* than it would be if

negligible apertures were used. The switch being ON longer results in *non*-neglgible energy being transferred to the capacitor 5310. This is the way in which "*pulse widths [] are established to improve energy transfer* from said input signal to said down-converted image."

For the foregoing reasons, the term is *not* indefinite and should be given its plain and ordinary meaning.

F. "means for under-sampling" (claim 6)

ParkerVision's Construction	Intel's Construction
Function: under-sampling an input signal to produce an input sample of a down-converted image of the input signal and under-sampling the input signal according to a control signal Structure: switch 2650 in Fig. 26; switch 5308 in Figs. 53A/53A-1; and equivalents thereof	Function: under-sampling an input signal to produce an input sample of a down-converted image of said input signal and under-sampling said input signal according to a control signal Structure: the switch 2650 and the capacitor 2652 in Fig. 26 and described at 26:1-27:21 and 28:20-28 and equivalents thereof.

The parties agree that the claims recite *two* functions performed by the "means for under-sampling." But the parties disagree on the structure that performs these functions. As discussed below, a *switch* is the *only* component that performs *each* of these functions.

Intel attempts to include a capacitor as part of the structure. But as discussed below, a capacitor does *not* perform *either* of the recited functions and, thus, is *not* part of the claimed structure. *See Northrop Grumman Corp. v. Intel Corp.*, 325 F.3d 1346, 1352 (Fed. Cir. 2003) ("Features that do not perform the recited function do not constitute corresponding structure and thus do not serve as claim limitations."); *Asyst Techs., Inc. v. Empak, Inc.*, 268 F.3d 1364, 1371 (Fed. Cir. 2001) ("The corresponding structure to a function set forth in a means-plus-function limitation *must actually perform the recited function*, not merely enable the pertinent structure to operate as intended . . . .").

Intel also seeks to improperly *exclude* the switches of Figures 53A and 53A-1 as structures

of the "means for under-sampling." But as discussed below, Intel's reason for doing so is based on a position this Court *already rejected* after briefing and oral argument in the 108 case.

First, Intel's construction is wrong because it seeks to *limit* the structure to an embodiment of a sample-and-hold system that under-samples using negligible apertures (Figure 26), while *excluding* an embodiment of an energy transfer system that under-samples using *non*-negligible apertures (Figures 53A, 53A-1). *See* '706 patent, 32:9-18. Intel's reasons for doing so is its view that "under-sampling" is not performed by an energy transfer system; it is only performed by a sample-and-hold system. But this Court already rejected Intel's position when the Court declined to limit the construction of "under-sampling" to sampling using negligible apertures. *See* Ex. 1 at 3. As such, contrary to Intel's construction, the structure of "means for under-sampling" should include the switch of Figures 53A and 53A-1, which are energy transfer system embodiments.

Second, Intel's construction is wrong because Intel tries to add a *capacitor* as part of the structure of a "means for under-sampling." But claim 6 of the '706 patent recites: "*means for under-sampling* an input signal to produce an input sample of a down-converted image of said input signal" and "*under-sampling means* under-samples said input signal according to a control signal." A *switch* is the *only* component that performs *either* function shown in red above.

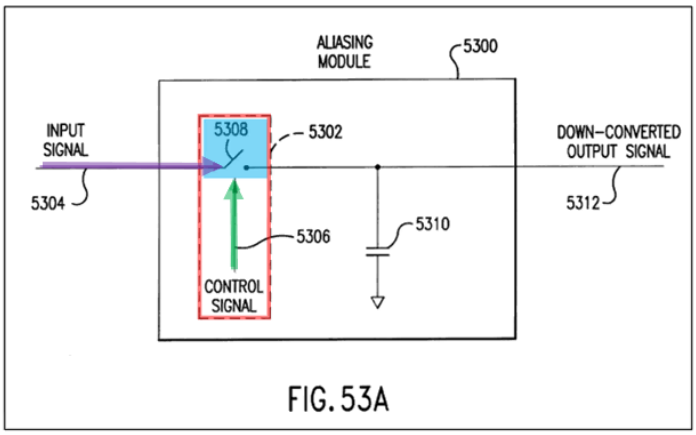


FIG. 53A

For example, Figure 53A of the '706 patent, above, illustrates a universal frequency

translation (UFT) module 5302 (red) having a switch 5308 (blue) controlled by a control signal 5306 (green arrow). The module 5302 receives an input signal 5304 (purple arrow), which is down-converted by under-sampling[14] the input signal. '706 patent, 28:44-46. Under-sampling of the input signal occurs by the *switch* being turned ON (closed) when the switch receives control signal 5306 (green) and OFF (opened) when the switch stops receiving the control signal. Thus, under-sampling "according to a control signal" occurs by the successive opening and closing of the switch.

The capacitor, on the other hand, merely *receives* a signal and its energy from the opening and closing of the switch. As such, the capacitor 5310 itself does *not* perform the function of under-sampling the input signal. Thus, contrary to Intel's construction, a capacitor is *not* part of the structure used for under-sampling the input signal for purposes of Section 112, ¶ 6. *See Northrop*, 325 F.3d at 1352.

Finally, Intel's citation to column/line numbers is not only unnecessary, but wrong. Citation to figures numbers alone is sufficient to identify the claimed structure. Once provided with relevant figures, the experts can determine the corresponding disclosure to argue structural equivalents. Intel, however, proposes a *narrow* set of column/line numbers to improperly restrict the equivalents analysis. For example, with regard to the switch 2650 of Figure 26, Intel cites to the '706 patent at "[col.] 26:1- [col.] 27:21 and [col.] 28:20-28." But the switch is also described at col. 29:4-8 and col. 39:25-28. Indeed, Intel omits all of the discussion of Figure 26 in col. 24:40 to col. 25:67, which provides context for the type of switches that can be used as equivalents of the disclosed switch 2650. Accordingly, Intel's recitation of column and lines

[14] The Court has defined "under-sampl[ing]" as "sampling at less than or equal to twice the frequency of the input signal." Ex. 1 at 3.

numbers should be rejected.

For the foregoing reasons, Intel's construction should be rejected and ParkerVision's construction should be adopted.

G. "first delaying means" (claim 6)

ParkerVision's Construction	Intel's Construction
Function: delaying the input sample of a down-converted image of said input signal Structure: capacitor 2656 in Fig. 26 or capacitor 5310 in Figs. 53A/53A-1; and equivalents thereof	Function: delaying said input sample Structure: the switch 2654 and capacitor 2656 shown in Fig. 26 and described at 25:57-27:21 and 28:20-28; and equivalents thereof.

The parties disagree on the function and structure of the "first delaying means." Claim 6 recites "an input sample of a down-converted image of said input signal" and the "first delaying means for delaying *said input sample*." As such, the function of the "first delaying means" is "delaying the input sample *of a down-converted image of said input signal*" as set forth in ParkerVision's construction. As discussed in Section V.B above, Intel's construction of "said input sample" improperly *omits* "*of a down-converted image of said input signal*" from the claimed function.

With regard to the structure, as discussed below, a *capacitor* is the component that performs the claimed function. Intel attempts to include a switch as part of the structure. But as discussed below, a switch does *not* perform the recited function and, thus, is *not* part of the claimed structure. *See Northrop*, 325 F.3d at 1352; *Asyst Techs.*, 268 F.3d at 1371.

Intel also seeks to improperly *exclude* the capacitor of Figures 53A and 53A-1 as structures of the "first delaying means." As discussed below, however, Intel's reason for doing so is based on a position *already rejected* by this Court in related Case No. 6:20-cv-00108.

First, Intel's construction is wrong because, yet again, it seeks to *limit* the structure to an

embodiment of a sample-and-hold system that under-samples using negligible apertures (Figure 26), while *excluding* an embodiment of an energy transfer system that under-samples using *non*-negligible apertures (Figures 53A, 53A-1). *See* '706 patent, 32:9-18. Intel's reasons for doing so is its view that "under-sampling" is not performed by an energy transfer system; it is only performed by a sample-and-hold system. But this Court has already rejected Intel's position when the Court declined to limit the construction of "under-sampling" to sampling using negligible apertures. *See* Ex. 1 at 3. As such, contrary to Intel's construction, the structure of "first delaying means" should include the capacitors of Figures 53A and 53A-1, which are energy transfer system embodiments.

Second, Intel's construction is wrong because Intel seeks to add a *switch* as part of the structure of a "first delaying means." Claim 6 of the '706 patent recites: "produc[ing] an input sample of a down-converted image of said input signal" and "first delaying means for *delaying said input sample*." A *capacitor* is the component that performs the function of "delaying said input sample" (i.e., delaying the input sample of a down-converted image of said input signal).

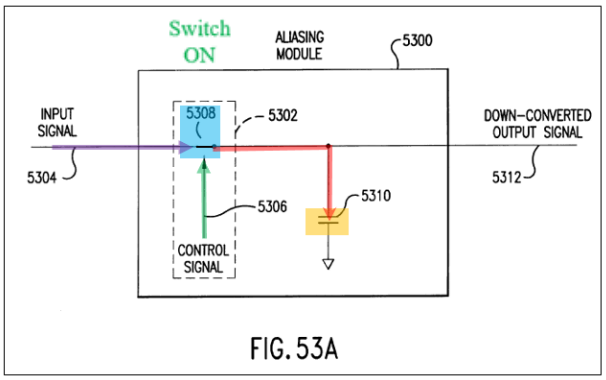


FIG. 53A

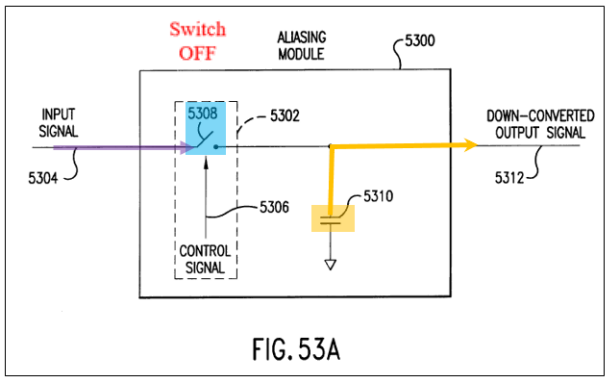


FIG. 53A

For example, Figure 53A (above left) of the '706 patent, above, illustrates an *input signal* 5304 (purple arrow), switch 5308 (blue) and capacitor 5310 (orange). Turning the switch ON (closing the switch by sending a control signal) and OFF (opening the switch when there is no control signal) creates an "input sample of a down-converted image of said *input signal*." Each

time the switch is turned ON and OFF, another "input sample of a down-converted image of said *input signal*" is created.

The capacitor receives input samples from the switch and is the component that is responsible for *delaying* the input samples. In particular, the input sample (red arrow) is sent to capacitor 5310 where it is stored (*delayed*) until, as shown in Figure 53A (above right), the switch 5308 turns OFF (opens) and the switch discharges energy (orange arrow). As such, the capacitor is the structure that delays the input sample. The switch 5308 itself does *not* perform the function of delaying the input sample. *See Asyst Techs.*, 268 F.3d at 1371 ("The corresponding structure to a function set forth in a means-plus-function limitation *must actually perform the recited function*, not merely enable the pertinent structure to operate as intended . . . ."). Thus, contrary to Intel's construction, a switch is *not* part of the structure used for delaying the input sample for purposes of Section 112, ¶ 6.

Finally, Intel's citation to column/line numbers is not only unnecessary, but wrong. Citation to figures numbers alone is sufficient to identify the claimed structure. Once provided with relevant figures, the experts can determine the corresponding disclosure to argue structural equivalents. Once again, Intel proposes a *narrow* set of column/line numbers to improperly restrict the equivalents analysis. For example, with regard to capacitor 2656 of Figure 26, Intel cites to "[col.] 25:57 - [col.] 27:21 and [col.] 28:20-28." Intel omits the discussion of Figure 26 in column 24, line 40 to column 25, line 56, which provides context for structure that can be used to determine equivalents. Accordingly, Intel's recitation of column and lines numbers should be rejected.

For the foregoing reasons, Intel's construction should be rejected and ParkerVision's construction should be adopted.

H. "second delaying means" (claim 6)

ParkerVision's Construction	Intel's Construction

Function: delaying instances of an output signal Structure: delay modules 1722A, 1722B, 1722C in Fig. 17; delay modules 1912, 1914 in Fig. 19; delay modules 2316, 2318 in Fig. 23; first delay module 2628, second delay module 2630 in Fig. 26; delay module 3204 shown in Fig. 32; sample and hold circuits 4501, 4503 shown in Fig. 45; analog delay line 3404 shown in Fig. 34 having a combination of capacitors, inductors, and/or resistors; and equivalents thereof	Function: delaying instances of an output signal Structure: structure including "first delay module 2628," "second delay module 2630" shown in Fig 26, "delay module 3204" shown in Fig. 32 and described at 35:1-18; the sample and hold circuits 4501 and 4503 in Fig. 45 and described at 32:44-64; or an analog delay line having a combination of capacitors, inductors and resistors described at 35:19-27; and equivalents thereof that operate to delay samples/instances of a signal presented at its input by a known amount.

The parties agree on the function performed by the "second delaying means," but disagree on the corresponding structure. The dispute over the corresponding structure relates to (1) Intel's attempt to *limit* the "and equivalents thereof" language to "operates to delay samples/instances of a signal presented at its input by a known amount," (2) ParkerVision's inclusion of the delay modules of Figures 17, 19 and 23, (3) the analog delay line, and (4) Intel's citations to column and line numbers from the specification to limit the structural equivalents.

Dispute 1: It is a fundamental principle that the structure of a means-plus-function term includes any equivalents. When defining the structure, this concept is captured by using "and equivalent thereof" or words to that effect. But Intel seeks to improperly narrow the "equivalents" of *all* structures of delay modules by injecting an *additional* limitation – "that operates to delay samples/instances of a signal presented at its input by a known amount." Through its construction, Intel is seeking to affect the experts' ability to argue equivalents – by narrowing the claimed structure, Intel effectively seeks to alter the scope of equivalents.

Indeed, as set forth below, through its construction of the *structure*, Intel is attempting to *re-write* the recited *function*, which the parties agree is "delaying instances of an output signal." But structure and function must be dealt with separately. *See JVW Enters. v. Interact*

Accessories, Inc., 424 F.3d 1324, 1330 (Fed. Cir. 2005) ("The district court's second construction confuses function with structure. Determining a claimed function and identifying structure corresponding to that function involve distinct, albeit related, steps that must occur in a particular order.").

In particular, instead of just reciting "and equivalents thereof" or words to that effect, Intel's definition of structure recites *functional* language "and equivalents thereof *that operate to delay samples/instances of a signal presented at its input by a known amount*." Intel takes this language from the specification: *"[a]s indicated above*, a delay module operates to delay samples/instances of a signal presented at its input by a known amount." '706 patent, 32:27-29. But Intel's additional language nonetheless is wrong. *First*, the "as indicated above" language is referring to *embodiments* discussed earlier in the specification. *Second*, Intel's language "operates to delay samples/instances of a signal presented at its input by a known amount" does *not* describe the structure but, rather, pertains to a *function* of a delay module. As such, Intel's equivalent language should be rejected.

Dispute 2: The delay modules 1722A, 1722B, 1722C in Figure 17, delay modules 1912, 1914 in Figure 19, and delay modules 2316, 2318 in Figure 23 *all* perform the claimed function of "delaying instances of an output signal." As such, all of these modules should be included as disclosed structures of the "second delaying means."

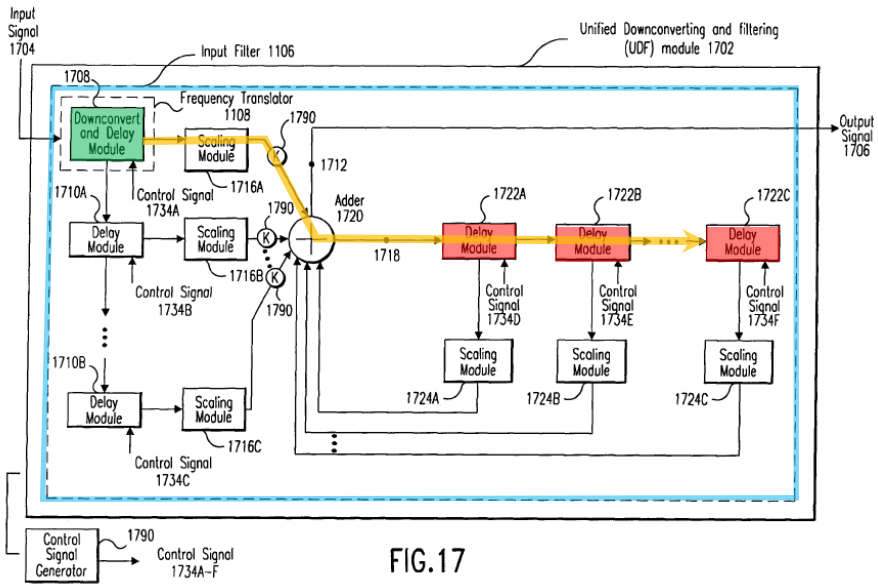


FIG.17

Claim 6 of the '706 patent recites "a filter, comprising . . . second delaying means for delaying instances of an output signal." As shown above in Figure 17, for example, the input filter 1106 (blue) comprises delay modules 1722A, 1722B, 1722C (red). The down converted and delay module (green) transmits an output signal (orange arrow), which will be delayed as it passes through each delay module 1722A, 1722B, 1722C (red).

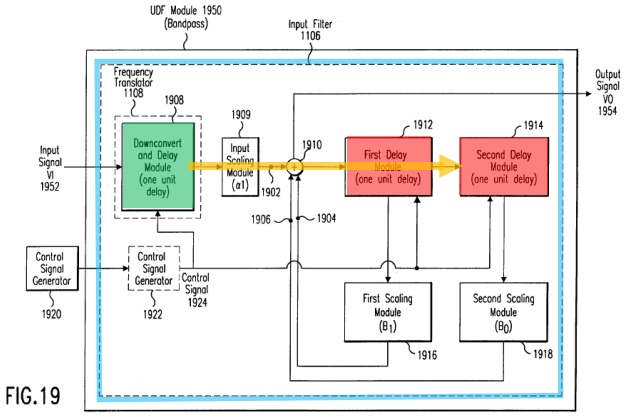


FIG.19

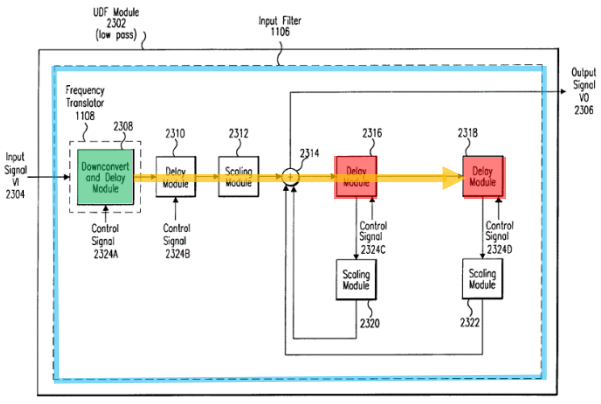


FIG.23

Figures 19 and 23 also show down-convert and delay modules 1908, 2308 (green) transmitting an output signal (orange arrow), which will be delayed as it passes through each delay module 1912, 1914 and 2316, 2318, respectively.

Indeed, based on Intel's own construction, Intel agrees that "delay modules" are "second delaying means." But Intel seeks to improperly *exclude* the delay modules of Figures 17, 19 and 23. According to Intel, the delay modules in these figures are "black boxes" that do not provide structural details and, thus, the delay modules of Figures 17, 19 and 23 cannot be included as disclosed structures.[15] Intel is wrong. These modules are *not* black boxes. Intel has simply chosen to ignore that there is an entire section in the specification (Section 3.4.2.2), which describes exemplary structures of the delay modules of Figures 17, 19 and 23, using Figure 17 as an illustration. *See* '706 patent, 34:60-35:31. As such, the claimed structure should include the delay modules of Figures 17, 19 and 23 and their connections to other components.

Dispute 3: The parties agree that an analog delay line is one of the claimed structures. And, the parties take their language regarding analog delay line from the same part of the specification.

> The *delay modules 1710, 1722 can also each be implemented using an analog delay line, such as the analog delay line 3404 in FIG. 34*, for example. As will be apparent to persons skilled in the relevant art(s), *an analog delay line 3404 is constructed using a combination of capacitors, inductors, and/or resistors*.

'706 patent, 35:19-24. ParkerVision's construction follows this language. Intel's language, on the other hand, suspiciously removes portions of this language. Intel does this to narrow the scope of the claim. In particular, unlike other structures that Intel identifies by figure and reference number, Intel omits analog delay line "3404 shown in Fig. 34." And whereas the specification recites "a combination of capacitors, inductors, *and/or* resistors," Intel's construction changes "and/or" to "or." As such, Intel's language should be rejected.

Dispute 4: Intel's citation to column/line numbers is not only unnecessary, but wrong as citation to figures numbers alone is sufficient to identify the claimed structure. Once provided

[15] Intel raised the "black box" argument for numerous terms during the parties' meet-and-confers as the basis for not agreeing to ParkerVision's constructions.

with relevant figures, the experts can determine the corresponding disclosure to argue structural equivalents. But yet again, Intel proposes a *narrow* set of column/line numbers to improperly restrict the equivalents analysis.[16] For example, with regard to sample and hold circuits 4501 and 4503 shown in Figure 45, Intel only cites to "[col.] 32:44-64." The description of the structure related to these circuits, however, are also described from col. 32:65 – col. 34:59. As such, Intel has *omitted several columns* of discussion regarding the structure of these circuits. Accordingly, Intel's recitation of column and lines numbers should be rejected.

For the foregoing reasons, Intel's construction should be rejected and ParkerVision's construction should be adopted.

I. "integral filter/frequency translator" (claim 28)

ParkerVision's Construction	Intel's Construction
"a circuit having a unified input filter and frequency translator"	Function: to filter and down-convert an input signal Structure: the Unified Downconvert and Filter (UDF) Module 2622 that includes: (1) the frequency translator 1108 having the down convert and delay module 2624; (2) a first delay module, including the delay module 2628 shown in Fig. 26, the delay module 3204 shown in Fig. 32 and described at 35:1-18, the sample and hold circuit 4501 or 4503 shown in Fig. 45 and described at 32:44-64, or the analog delay line having a combination of capacitors, inductors and/or resistors described at 35:19-27 that operates to delay samples/instances of a signal presented at its input by a known amount; (3) a second delay module including the delay module 2630 shown in Fig. 26, the delay module 3204 shown in Fig. 32 and described at 35:1-18, the sample and hold circuit 4501 or 4503 shown in Fig. 45 and described at 32:44-64, or the analog delay line having a combination of capacitors, inductors and/or resistors described at 35:19-27 that operates to delay samples/instances of a signal presented at its input by a known amount; (4) a first scaling module, including the first scaling module 2632 shown in Fig. 26, the resistor attenuator 3602 shown in Fig. 36 and described at 35:44-55, or the

[16] Intel is also inconsistent when it chooses to include column and lines numbers. For example, for Figure 26, Intel provides no citations.

	amplifier/attenuator 3704 implemented using operational amplifiers, transistors, or FETs shown in Fig. 37 and described at 35:60-67; (5) a second scaling module, including the second scaling module 2634 shown in Fig. 26, the resistor attenuator 3602 shown in Fig. 36 and described at 35:44-55, or the amplifier/attenuator 3704 implemented using the operational amplifiers, transistors, or FETs shown in Fig. 37 and described at 35:60-67; (6) a first adder including, the adder 2625 in Fig. 26, adder 1720 in Fig. 17, the adder 2522 in Fig. 25, the summer 3902 in Fig. 39, or the summer 4102 in Fig. 41; and (7) a second adder, including the adder 2626 in Fig. 26, adder 1720 in Fig. 17, the adder 2522 in Fig. 25, the summer 3902 in Fig. 39, and the summer 4102 in Fig. 41; and equivalents thereof.

The term is straight-forward and simply refers to a circuit having a unified input filter and frequency translator. Despite the structural nature of a "filter" and "frequency translator," Intel asserts that the term implicates 35 U.S.C. §112, ¶ 6. Similar to its position on other non-means terms discussed above, Intel is incorrect. Once again, the term does *not* use the word "means." Thus, there is a presumption that §112, ¶ 6 does *not* apply. *Williamson,* 792 F.3d at 1348. And the claims recite a definite structure. Indeed, the claims do not simply recite a "module" or "circuit," but recite a specific type of structure – a filter and frequency translator.

A "filter" has a known structure that incorporates components/circuits such as "capacitors, inductors, resistors." *See e.g.,* '706 patent, 38:64-66 ("The fabrication of *filters* typically requires very tight tolerances on *component parts of the filters, such as capacitors, inductors, resistors*, etc."). A "frequency translator" also has a known structure that incorporates components/circuits such as a switch and storage element (capacitor). *See e.g.,* '706 patent, claims 3 ("a *frequency translator*, comprising a *down-convert and delay module* . . . wherein said *down-convert and delay module comprises a switch and a storage element*, wherein a first node of said storage element is coupled to a node of said switch, and a second node of said storage element is coupled to a reference potential.").

The specification explains that an "integrated" filter and frequency translator simply means that the filter and frequency translator are structurally "unified" so that their operations – filtering/frequency selection and frequency translation – are performed "concurrently." *See, e.g., id.* at 13:53-58.

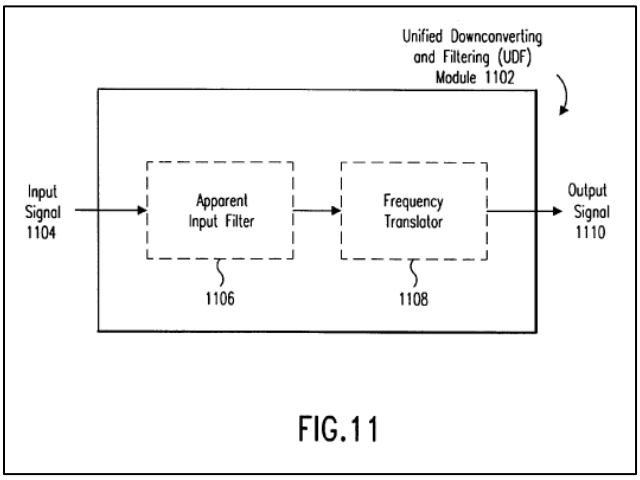


FIG.11

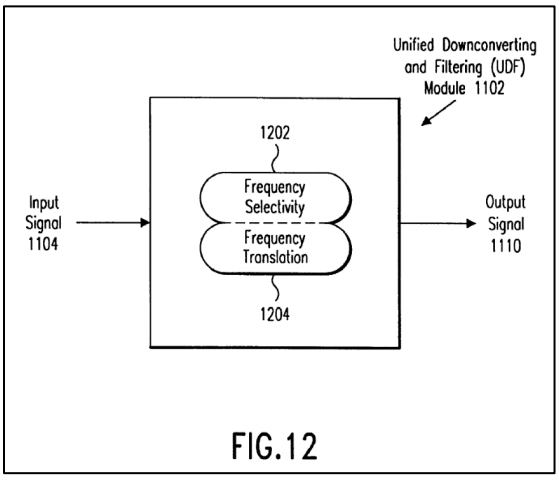


FIG.12

In particular, Figures 11 and 12 above illustrate a unified downconverting and filtering module 1102. The specification describes this component as having integrated/unified filtering/frequency selection and frequency translation.

> In practice, the *input filtering operation performed by the UDF module 1102 is integrated with the frequency translation operation*. The *input filtering operation can be viewed as being performed concurrently with the frequency translation operation*. This is a reason why the input filter 1106 is herein referred to as an "apparent" input filter 1106.
>
> * * * *
>
> Specifically, according to the present invention, the UDF module 1102 performs the *frequency selectivity operation and the frequency translation operation as a single, unified (integrated) operation*. This is conceptually represented in FIG. 12, where *the selectivity operation 1202 is shown as being combined or integrated with the frequency translation operation 1204*. This is also indicated via the dotted line representations of the apparent input filter 1106 and the frequency translator 1108 in FIG. 11.

'706 patent, 13:53-58; 14:40-48.

For the foregoing reasons, the term is *not* subject to §112, ¶ 6[17] and it should be given its plain and ordinary meaning.

J. "frequency translator" (claim 34)

ParkerVision's Construction	Intel's Construction
Not means-plus-function Plain and ordinary meaning	Function: produce a sample of a down-converted image of an input signal, and to delay said sample Structure: the down convert and delay module 2624 in Fig. 26 and described at 26:1-27:21 and 28:20-41, that includes the switches 2650 and 2654, the scalers 2690A and 2690B, and the capacitors 2652 and 2656; and equivalents thereof.

The term is straight-forward and does not require a construction. Despite the structural nature of a "frequency translator," Intel asserts that the term implicates 35 U.S.C. §112, ¶ 6. Similar to its position on other non-means terms discussed above, Intel is incorrect. Once again, the term does *not* use the word "means." Thus, there is a presumption that §112, ¶ 6 does *not* apply. *Williamson,* 792 F.3d at 1348. And the claims recite a definite structure. Indeed, the claims do not simply recite a "module" or "circuit," but recite a specific type of structure – "a *frequency* translator." A "*frequency* translator" has a known structure that incorporates components/circuits such as a switch and storage element (capacitor).

Indeed, dependent claim 186, which depends from claim 34, makes it clear that the

[17] Even if §112, ¶ 6 applies (which it doesn't), Intel's construction is wrong. *First*, Intel's construction is missing one of the functions of the "integral filter/frequency translator" set forth in the claim – "under-sampl[ing] said input signal according to a control signal." '706 patent, 48:1-2. *Second*, even assuming that the "integral filter/frequency translator" is limited to the Unified Downconvert and Filter (UDF) Module as Intel asserts, Intel's construction is still missing relevant structures. Intel seeks to *limit* the structure to a specific embodiment based on Figure 26. But Intel's construction of the structure is missing the structures in Figures 11, 12, 17, 19, 23, 30, 53A, and 53A-1.

"*frequency* translator" includes such structural components/circuits. And the dependent claims must be considered in determining the applicability of § 112, ¶ 6. *See, e.g., TEK Global*, 920 F.3d at 785. In particular, dependent claim 186 not only discloses the structural components/circuits of the "*frequency* translator" – switch and storage module (capacitor) – but also describes their *physical* connection: " said frequency translator comprises: a switch; and a storage module electrically coupled to said switch." '706 patent, 60:51-52. Thus, the presumption *against* §112, ¶ 6 stands. *See TEK Global*, 920 F.3d at 786.

For the foregoing reasons, the term is *not* subject to §112, ¶ 6[18] and it should be given its plain and ordinary meaning.

K. "energy transfer signal comprising a train of pulses" (claims 106, 176)

ParkerVision's Construction	Intel's Construction
"a signal comprising a train of pulses having non-negligible apertures that tend away from zero"	"a signal comprising (i.e., that includes) a train of pulses having non-negligible apertures that tend away from zero"

The parties' constructions are nearly identical. The only difference relates to the term "comprising." Intel seeks to narrowly limit the term "comprising" – "(i.e., that includes)" to further a non-infringement position. But "comprising" is readily understandable by a jury and

[18] Even if §112, ¶ 6 applies (which it doesn't) Intel's construction is wrong. *First*, Intel's construction is missing one of the functions of the "frequency translator" set forth in the claim – "under-sampl[ing] said input signal according to a control signal." '706 patent, 48:56-57. *Second*, Intel's construction is missing relevant structures of the "frequency translator." Intel seeks to *limit* the structure to an embodiment of a system that under-samples using negligible apertures (Figure 26), while *excluding* embodiments that under-sample using *non*-negligible apertures (e.g., Figures 53A, 53A-1). Intel repeatedly resorts to this tactic. Intel's reasons for excluding the *non*-negligible apertures embodiments is its view that "under-sampling" is performed only using negligible apertures. But after briefing and oral arguments at the hearing, this Court has already rejected Intel's position in the 108 case. The Court declined to limit the construction of "under-sampling" to sampling using negligible apertures in the Court's January 28, 2021 Claim Construction Order. *See* Ex. 1 at 3. As such, Intel's construction of the structure is missing at least the aliasing modules 5300 of Figures 53A, 53A-1.

does not require clarification. Indeed, "comprising" has a number of different meanings: "to consist of; be composed of"; "to include; contain." Ex. 4, The American Heritage College Dictionary (3d ed. 1997) at 286. While "comprising" certainly can mean "includes," it has other meanings as well.

For the foregoing reasons, Intel's "(i.e., that includes)" language should be rejected and ParkerVision's construction should be adopted.

L. "modulated signal" (claim 127)

ParkerVision's Construction	Intel's Construction
"an electromagnetic signal at a transmission frequency having at least one characteristic that has been modulated by a baseband signal."	"a signal with one or more physical characteristics varied to represent the information to be transmitted"

In the parties' related 108 case, the Court construed "modulated carrier signal" as "an electromagnetic signal at a transmission frequency having at least one characteristic that has been modulated by a baseband signal." *See* Ex. 1 at 6. The wireless receiver technology in the 108 case is the *same* technology disclosed in the '706 patent in this case and, thus, "modulated signal" has the same meaning as "modulated carrier signal." As such, the construction of "modulated signal" in this case should be consistent with the construction of "modulated carrier signal" in the 108 case. Accordingly, ParkerVision's construction adopts the Court's prior construction.

Intel, on the other hand, seeks a second bite at the apple and to *re-argue* the term. Tellingly, Intel's construction of "modulated carrier signal" in the 108 case included that the signal is "modulated by a baseband signal." But here, Intel omits this language. Nevertheless, Intel's construction is wrong. *First*, though the term for construction is "modulated signal," Intel's construction is taken from the specification's description of "modulation" (a *process*):

"*[t]he process of varying* one or more physical characteristics of a signal to represent the information to be transmitted." '706 patent, 9:58-60. *Second*, Intel's language – "information *to be* transmitted" – pertains to a signal/information that has *not yet been* transmitted. But claim 127 of the '706 patent, which contains the disputed term, pertains to a signal that has *already* been transmitted. Specifically, claim 127 recites "said *input signal* is a modulated signal." An "*input* signal" refers to a signal that has been *received* by a wireless device. In other words, contrary to Intel's construction, as an *input* signal, a modulated signal has *already* been transmitted over the air and, thus, should be "at a transmission frequency" as set forth in ParkerVision's construction.

For the foregoing reasons, Intel's construction should be rejected and ParkerVision's construction, which adopts this Court's prior construction, should be adopted.

M. "filter tuning means" (claims 134)

ParkerVision's Construction	**Intel's Construction**
Function: tuning one or more filter parameters Structure: scaling modules 1716A, 1716B, 1716C, 1724A, 1724B, 1724C in Fig. 17; control signal generator 1790 in Fig. 17; input scaling module 1909 in Fig. 19; scaling modules 1916, 1918 in Fig. 19; scaling modules 2312, 2320, 2322 in Fig. 23; scaling module 2632, 2634 in Fig. 26; scaling module 3502 including resistor attenuator 3504, 3602 in Figs. 35, 36; scaling module 3702 including amplifier/attenuator 3704 in Fig. 37; control signal generator 4202 in Fig. 42; and equivalents thereof	Function: tuning one or more filter parameters Structure: scaling modules including the resistor attenuator 3602 (shown in Fig. 36 and described at 35:44-55) or the amplifier/attenuator 3704 implemented using operational amplifiers, transistors, or FETS (shown in Fig. 37 and described at 35:60-67), each of the resistor attenuator 3602 and the amplifier/attenuator 3704 having tunable resistors, capacitors, or inductors (as described at 42:33-36); and equivalents thereof; OR the control signal generator 4202 (shown in Fig. 42 and described at 36:44-62) implemented with a tunable oscillator 4204 and an aperture optimizing module 4210 using tunable components (such as tunable resistors, capacitors, inductors, etc.) (described at 36:63-37:5 and 42:27-32) and equivalents thereof.

The parties agree on the function the "filter tuning means" performs, but disagree on the corresponding structure. The dispute regarding the structure relates to (1) ParkerVision's

inclusion of the scaling modules of Figures 17, 19, 23 and 26, (2) ParkerVision's inclusion of "scaling module 3502 including resistor attenuator 3504" in Figure 35, (3) Intel *limiting* the amplifier/attenuator 3704 to being "implemented using operational amplifiers, transistors, or FETS," (4) Intel *limiting* resistor attenuator 3602 and the amplifier/attenuator 3704 to "having tunable resistors, capacitors, or inductors," (5) Intel's *limiting* control signal generator 4202 to being "implemented with a tunable oscillator 4204 and an aperture optimizing module 4210 using tunable components (such as tunable resistors, capacitors, inductors, etc.)," and (6) Intel's citations to column and line numbers from the specification.

Dispute 1: Scaling modules 1716A, 1716B, 1716C, 1724A, 1724B, 1724C in Fig. 17; control signal generator 1790 in Fig. 17; input scaling module 1909 in Fig. 19; scaling modules 1916, 1918 in Fig. 19; scaling modules 2312, 2320, 2322 in Fig. 23; scaling module 2632, 2634 in Fig. 26 (shown in red below) *all* perform the claimed function of "tuning one or more filter parameters." As such, *all* of these components should be included as disclosed structures of the "filter tuning means."

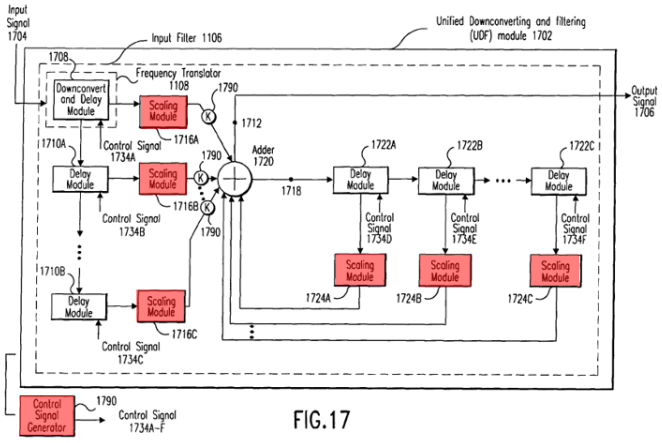


FIG.17

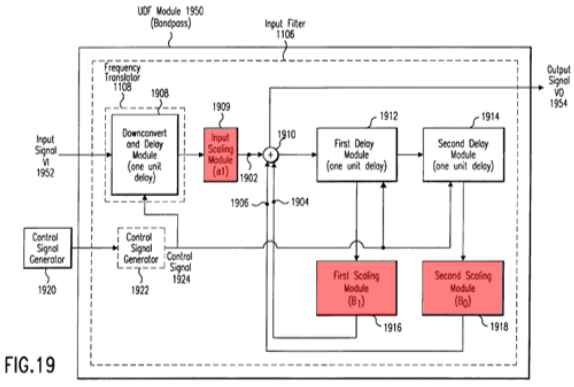


FIG.19

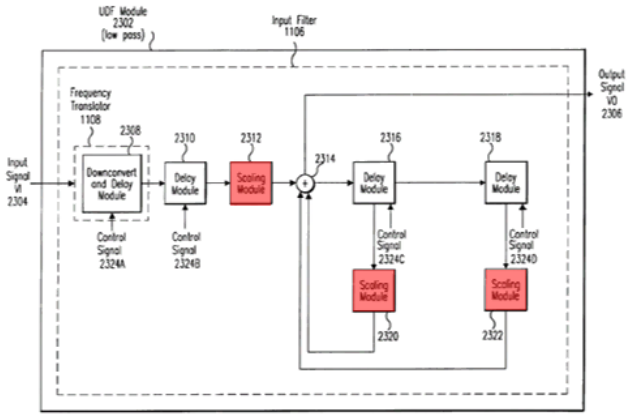


FIG.23

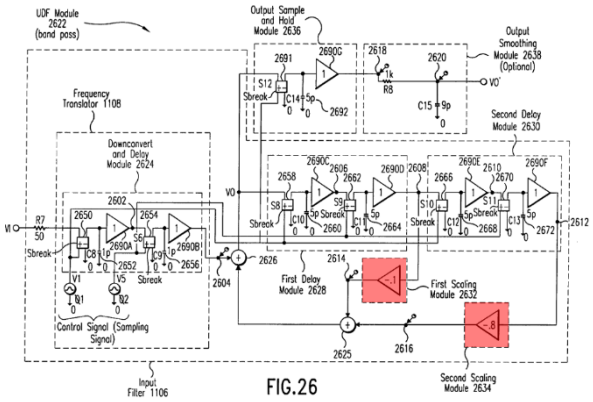


FIG.26

Indeed, based on Intel's own construction, Intel agrees that "scaling modules" and "control signal generators" are "filter tuning means." But Intel seeks to improperly *exclude* the scaling modules and control signal generators of Figures 17, 19, and 23.[19] According to Intel, the scaling modules and control signal generator in these figures are "black boxes" that do not provide structural details and, thus, the scaling modules and control signal generator of Figures 17, 19, and 23 cannot be included as disclosed structures. Intel is wrong. These components are *not* black boxes. Intel has simply chosen to ignore that there are entire sections in the specification (Sections 3.4.2.3 and 3.4.2.5), which describe exemplary structures of the scaling modules and control signal generator of Figures 17, 19, and 23 using Figure 17 as an illustration. *See* '706 patent, 35:33-67; 36:35-37:9. As such, the claimed structure should include the scaling modules and control signal generator of Figures 17, 19, 23 and 26, and their connections to other components.

Dispute 2: The scaling module 3502 of Figure 35 (below), which includes resistor attenuator 3504, also performs the claimed function of "tuning one or more filter parameters." As

[19] Intel also excludes the structures in Figure 26. ParkerVision is not aware of the bases for this exclusion and will respond to Intel's argument in ParkerVision's Reply Brief.

such, the "scaling module 3502 including resistor attenuator 3504" of Figure 35 should be included as a disclosed structure of the "filter tuning means."

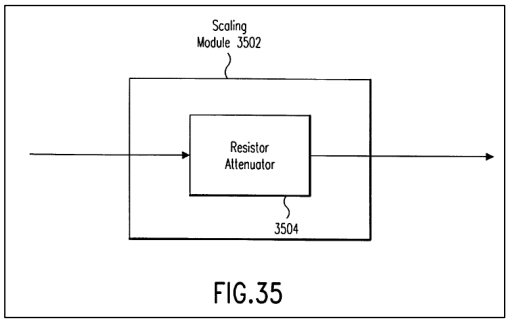


FIG.35

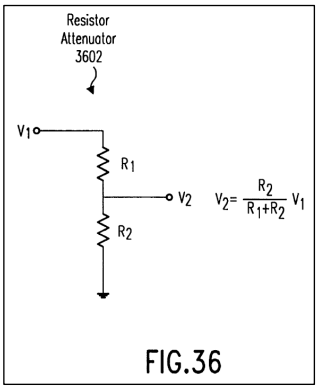


FIG.36

As shown above, Figure 35 illustrates a scaling module 3502 with a resistor attenuator 3504. Figure 36 discloses an *exemplary* embodiment of the resistor attenuator 3602.

Indeed, based on Intel's own construction, Intel agrees that a scaling module with a resistor attenuator is a "filter tuning means." But Intel seeks to include only the resistor attenuator 3602 and improperly *exclude* the scaling module 3502 and resistor attenuator 3504 of Figure 35. According to Intel, the scaling module and resistor attenuator of Figure 35 are "black boxes" that do not provide structural details and, thus, Figure 35 cannot be included as a disclosed structure. Intel is wrong. *First*, as discussed above, these modules are *not* black boxes. Intel has simply chosen to ignore that there is an entire section in the specification (Section 3.4.2.3), which describes exemplary structures of the scaling modules. *See* '706 patent, 35:33 – 36:4. *Second*, a *resistor* attenuator is a well-known structure that is made up of *resistors*. As such, the claimed structure should include "scaling module 3502 including resistor attenuator 3504" of Figure 35.

Dispute 3: The parties agree that the disclosed structure includes a scaling module having an amplifier/attenuator 3704. But then Intel drafted its construction in a way so that *all* embodiments of amplifier/ attenuator 3704 are "implemented using operational amplifiers,

transistors, or FETS." Through its construction, Intel is seeking to affect the experts' ability to argue equivalents – by narrowing the structure, Intel seeks to alter the scope of equivalents.

Intel's language is wrong. The specification makes it clear that only *some* embodiments of the amplifier/ attenuator 3704 are "implemented using operational amplifiers, transistors, or FETS": "*amplifiers* suitable for use as scaling modules 1716, 1724 in the UDF module 1702 *can be* implemented using a variety of circuit components, *such as, but not limited to*, *operational amplifiers (OP AMPS), transistors, FETS, etc.*" '706 patent, 35:63-67. So, while it is true that an amplifier/attenuator *can* be implemented with "operational amplifiers, transistors, or FETS," contrary to Intel's construction, *not all* embodiments of the amplifier/attenuator 3704 must be implemented using these components. As such, the claimed structure should *not* limit all amplifiers/attenuators to being "implemented using operational amplifiers, transistors, or FETS."

Dispute 4: The parties agree that the disclosed structure includes scaling modules having a resistor attenuator 3602 and scaling modules having an amplifier/attenuator 3704 in Figures 36 and 37. But in order to further a non-infringement theory, Intel seeks to improperly *limit* resistor attenuator 3602 and amplifier/ attenuator 3704 to having "tunable" components – "*tunable* resistors, capacitors, or inductors." Once again, through its construction, Intel is seeking to affect the experts' ability to argue equivalents – by narrowing the structure, Intel seeks to alter the scope of equivalents.

Again, Intel's language is wrong. *First*, Intel is attempting to read a limitation from dependent claim 138 into dependent claim 134. In particular, claim 134 recites "filter tuning means." Claim 138, which depends from claim 134, further recites: "wherein said filter tuning means comprises: *means for adjusting at least one scale factor*. . . ." And the specification discloses that the "means for adjusting at least one scale factor" of claim 138 is "adjustable

components, such as *tunable resistors, capacitors, inductors, etc."* '706 patent, 42:33-36 ("The *scaling factors can be adjusted* by implementing the scaling modules 1716, 1722 *using adjustable components, such as tunable resistors, capacitors, inductors, etc.*"). So, whereas "tunable" components are part of the "means for adjusting" of dependent claim 138, such "tunable" components should not be part of the *broader* independent claim 134, which merely recites "filter tuning means."

Second, Intel has drafted its construction in a way so that *all* embodiments of the resistor attenuator 3602 and amplifier/ attenuator 3704 have "*tunable* resistors, capacitors, or inductors." The specification, however, makes it clear that only *some* embodiments have "tunable resistors, capacitors, or inductors": "The scaling factors *can be* adjusted by implementing the *scaling modules 1716, 1722 using adjustable components, such as tunable resistors, capacitors, inductors, etc.*" '706 patent, 42:33-36. So, while it is true that a resistor attenuator 3602 or an amplifier/attenuator 3704 *can* have "tunable resistors, capacitors, or inductors," contrary to the way in which Intel drafted its construction, *not all* embodiments of the resistor attenuator 3602 and amplifier/attenuator 3704 must have these components. As such, the claimed structure should *not* limit all resistor attenuators and amplifiers/attenuators to "having tunable resistors, capacitors, or inductors."

Dispute 5: The parties agree that the disclosed structure includes the control signal generator 4202 in Figure 42. But in order to further a non-infringement theory, Intel *once again* seeks to improperly *limit* the structure to having "tunable" components. Here, Intel seeks to limit the control signal generator 4202 to being implemented with (1) "a *tunable* oscillator 4204" and (2) "an aperture optimizing module 4210 using *tunable* components (such as *tunable* resistors, capacitors, inductors, etc.)." Yet again, through its construction, Intel is seeking to affect the

experts' ability to argue equivalents – by narrowing the structure, Intel seeks to alter the scope of equivalents.

Contrary to Intel's language that the control signal generator 4202 is "implemented with a tunable oscillator 4204," the oscillator 4204 is *not* always a "tunable" oscillator. The specification broadly describes oscillator 4204 without the modifier "tunable": "[a]n *example* implementation of a control signal generator 1790 is presented in FIG. 42. The *control signal generator* 1790 *includes an oscillator 4204* . . . ." '706 patent, 36:47-50. The specification also describes a "tunable" oscillator as merely an *embodiment*: "The control signal *can be* adjusted, for example, by implementing the control signal generator 4202 (FIG. 42) *using a tunable oscillator* . . . ." *Id.* at 42:27-29. So, though a tunable oscillator *can* certainly be used, contrary to the way in which Intel's drafted its construction, *not all* embodiments of the oscillator must be tunable. As such, the claimed structure should *not* limit all control signal generators to generators including "tunable" oscillators.

Moreover, contrary to Intel's language that the control signal generator 4202 is "implemented with . . . an aperture optimizing module 4210 using *tunable* components (such as tunable resistors, capacitors, inductors, etc.)," as shown below, the aperture optimizing module (green) 4210 is described as an *optional* component as shown in red.

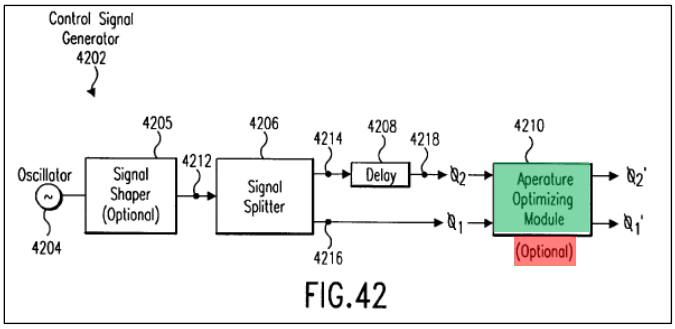


FIG.42

Even then, the specification makes it clear that the use of "tunable" components in an aperture optimizing module 4210 is merely one *embodiment*: "The control signal *can be* adjusted, for

example, by implementing the control signal generator 4202 (FIG. 42) *using a tunable oscillator, and implementing the aperature optimizing module 4210 using tunable components (such as tunable resistors, capacitors, inductors, etc.)*." '706 patent, 42:27-32. So, while "an aperture optimizing module 4210 using tunable components" *can* certainly be used, contrary to the way in which Intel's drafted its construction, *not all* embodiments of the control signal generator 4202 must include "an aperture optimizing module 4210 using tunable components." As such, the claimed structure should *not* limit all control signal generators to generators "implemented with . . . an aperture optimizing module 4210 using tunable components (such as tunable resistors, capacitors, inductors, etc.)."

Dispute 6: *Finally*, Intel's citation to column/line numbers is not only unnecessary, but wrong. As explained above, citation to figures numbers alone is sufficient to identify the claimed structure. Once provided with relevant figures, experts can determine the corresponding disclosure to argue structural equivalents. Again, Intel proposes a *narrow* set of column/line numbers to improperly restrict the equivalents analysis. For example, with regard to scaling modules, Intel's construction carefully *omits* column 35, lines 32-43, which provides a broad description of the scaling module. Accordingly, Intel's cherry-picked and limiting recitation of column and lines numbers should be rejected.

For the foregoing reasons, Intel's construction should be rejected and ParkerVision's construction should be adopted.

VI. U.S. Patent No. 7,050,508 – Disputed terms for construction

A. "pulse shaping means" (claim 1)

ParkerVision's Construction	Intel's Construction
Function: shaping a string of pulses from a reference signal Structure: pulse shaper 3900 in Fig. 39A; pulse	Function: shaping a string of pulses from a reference signal Structure: the pulse shaping circuit 3900

shaping circuit/pulse shaper 4000 in Fig. 40A; pulse shaping circuit 4100 in Fig. 41; harmonic enhancement module 4602 in Fig. 46; signal shaper 5010 in Fig. 50; harmonic enhancement module 5124 in Fig. 51B-C; pulse shaper 5310 in Fig. 53; pulse shaper 5438 in Fig. 54A; pulse shaper 5438 in Fig. 55; pulse shaper 5632 in Fig. 56; pulse shaping circuit 5722 in Fig. 57A-C, pulse shaper 6216 in Fig. 62; pulse shaper 7812 in Fig. 78; and equivalents thereof	shown in Fig. 39A and described at 48:8-39, the pulse shaping circuit 4000 shown in Fig. 40A and described at 48:40-49:5, and the pulse shaping circuit 4100 shown in Fig. 41 and described at 49:6-26; and equivalents thereof.

The parties agree on the function the "pulse shaping means" performs, but disagree on the corresponding structure.[20] Intel seeks to *exclude* the following structures: harmonic enhancement module 4602 in Fig. 46; signal shaper 5010 in Fig. 50; harmonic enhancement module 5124 in Fig. 51B-C; pulse shaper 5310 in Fig. 53; pulse shaper 5438 in Fig. 54A; pulse shaper 5438 in Fig. 55; pulse shaper 5632 in Fig. 56; pulse shaping circuit 5722 in Fig. 57A-C, pulse shaper 6216 in Fig. 62; pulse shaper 7812 in Fig. 78. *All* of these components, however, perform the claimed function of "shaping a string of pulses from a reference signal." As such, *all* of these components should be included as disclosed structures of the "pulse shaping means."

Indeed, based on Intel's own construction, Intel agrees that "pulse shapers," "pulse shaping circuits" and "harmonic enhancement modules" are "pulse shaping means." But, according to Intel, the "pulse shapers," "pulse shaping circuits" and "harmonic enhancement modules" of Figures 46, 50, 51B-C, 53, 54A, 55, 56, 57A-C, 62 and 78 are "black boxes" that do not provide structural details and, thus, cannot be included as disclosed structures. But as before, Intel is wrong.

These components are *not* black boxes. Intel has simply chosen to ignore that there are entire sections in the specification entitled "*Structural* Description" (Sections 4.2.1.2, 4.2.2.2,

[20] Intel's recitation of "pulse shaping circuit 3900" is *not* technically accurate. The specification refers to 3900 as "pulse shaper 3900," *not* "pulse shaping circuit." *See* '508 patent, 48:15, 20, 37.

4.2.3.2), which describe exemplary structures of "pulse shapers," "pulse shaping circuits" and "harmonic enhancement modules," using harmonic enhancement module 4602 as an illustration. *See* '508 patent, 46:65-47:7; 47:26-35; 47:45-52. Indeed, the "harmonic enhancement module 4602" is described as a "pulse shaper" and "pulse shaper circuit." *See id*. at 45:59-60 ("The *harmonic enhancement module (HEM) 4602* (FIG. 46) is also referred to as a '*pulse shaper*.'"); *id.* at 46:66-47:1 ("*harmonic enhancement module 4602*, herein after referred to as a *pulse shaping circuit* 4602."). And the specification describes "harmonic enhancement modules"/ "pulse shapers"/ "pulse shaping circuits" as having "*digital logic devices* that result in a string of pulses 4606 being output that has [] pulse[] for every pulse in the continuous periodic waveform 4604 . . . ." *Id*. at 47:3-6, 30-34. So not only would a skilled person know to use "digital" and "logic" devices as the structure instead of analog devices or something other than logic circuitry, but a skilled person would know to use "digital logic devices" "that result in a string of pulses 4606 being output that has one pulse for every pulse in the continuous periodic waveform 4604. . . ." As such, the claimed structure should include the "pulse shapers," "pulse shaping circuits" and "harmonic enhancement modules" of Figures 46, 50, 51B-C, 53, 54A, 55, 56, 57A-C, 62, 78.

Moreover, yet again, Intel's citation to column/line numbers is not only unnecessary, but wrong. Citation to figures numbers alone is sufficient to identify the claimed structure. Intel, however, wants to use column/line number to engage in gamesmanship. Yet again, Intel proposes a *narrow* set of column/line numbers to improperly restrict the equivalents analysis. For example, with regard to the "harmonic enhancement module 4602" of Figure 46, Intel's construction carefully *omits* col. 46:65 – col. 47:7, col. 47:26-35, and col. 47:45-52. Accordingly, Intel's recitation of column and lines numbers should be rejected.

For the foregoing reasons, Intel's construction should be rejected and ParkerVision's

construction should be adopted.

B. "aperture generation means" (claim 1)

ParkerVision's Construction	Intel's Construction
Function: generating a string of multiple pulses from said string of pulses Structure: aperture generation module 7806 in Fig. 78 having gate(s) and delay(s) such as the aperture generation module shown in Fig. 79; and equivalents thereof	Function: generating a string of multiple pulses from said string of pulses Structure: the aperture generation module 7806 shown in Fig. 79 and described at 49:54-50:5; and equivalents thereof.

The parties agree on the function the "aperture generation means" performs, but disagree on the corresponding structure. Intel seeks to exclude Figure 78. Once again, Intel asserts that Figure 78 is a "black box" that does not provide structural details and, thus, this component cannot be included as a disclosed structure.

But Intel is wrong. These modules are *not* black boxes. Aperture generation modules use structural components such as gate(s) and/or delay(s) to generate a string of multiple pulses. Figure 79 illustrates one *exemplary configuration* showing how those components are arranged. But instead of defining the structure by the components (gate(s) and delay(s)) that perform the recited function as it should do, Intel focuses its construction on the *specific configuration* of these components. This is no accident. Through its construction, Intel is seeking to affect the experts' ability to argue equivalents – by glossing over Figure 78 and narrowing the claimed structure to the *exact configuration* of Figure 79 having multiple delays connected to a specific type of gate (NOR gate), Intel seeks to alter the scope of equivalents. Though module 7086 in Figure 79 is certainly an embodiment of how a gate and delays can be arranged in an aperture generation module, contrary to Intel's construction, it is not the only configuration a gate(s) and delay(s) that performs the recited function.

Moreover, yet again, Intel's citation to column/line numbers is not only unnecessary, but

wrong. Citation to figures numbers alone is sufficient to identify the claimed structure. And once provided with relevant figures, the experts can determine the corresponding disclosure to argue structural equivalents. Again, Intel proposes a *narrow* set of column/line numbers to improperly restrict the equivalents analysis. For example, with regard to the aperture generation module 7806 of Figure 78 and 79, Intel omits the description set forth in col. 49:37-53, which describes the type of signal that needs to be processed by the aperture generations means – a string of pulses from a pulse shaper. The type of signal, in turn, affects how the components of the aperture generation means are configured. Accordingly, Intel's narrowing recitation of column and lines numbers should be rejected.

For the foregoing reasons, Intel's construction should be rejected and ParkerVision's construction should be adopted.

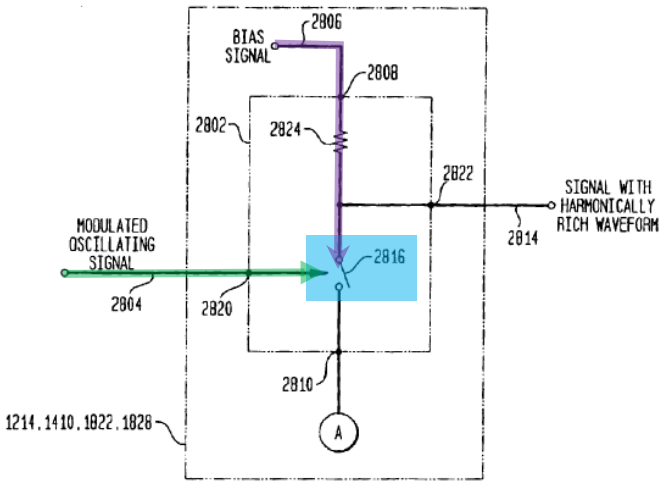
C. "gating means" (claim 1)

ParkerVision's Construction	**Intel's Construction**
Function: gating a bias signal under the control of said string of multiple pulses to generate a periodic signal having a plurality of harmonics at least one of which is at a desired frequency Structure: the switches shown in Fig. 28A, 29A, 30A, 31A, 32A, 33A, 53, 54A, 55, 56, 57A-C; and equivalents thereof	Function: gating a bias signal under the control of said string of multiple pulses to generate a periodic signal having a plurality of harmonics at least one of which is at a desired frequency Structure: the switch module 2802 shown in Fig. 28A and described at 35:14-36:24 and 45:47-46:37, the switch module 2802 shown in Fig. 29A and described at 36:25-50, and the switch module 2802 shown in Fig. 30A and described at 36:25-50 and equivalents thereof.

The parties agree on the function the "gating means" performs, but disagree on the corresponding structure. In particular, there are two disputes between the parties: (1) whether a "switch" (ParkerVision's construction) or "switch module" (Intel's construction) performs the claimed function; and (2) whether the structure includes the switches shown in Figures 31A, 32A, 33A, 53, 54A, 55, 56 and 57A-C.

Dispute 1: The parties agree that the function of the "gating means" is "gating a bias signal under the control of said string of multiple pulses." As such, the question is what component performs the function of "gating" a bias signal "under the control" of pulses. As set forth in Section VI.D below, the parties agree that "gating" relates to the opening and closing of a device. The *only* device that opens and closes is a *switch*. Moreover, the only device that is "under the control" of pulses is a *switch*.

FIG. 28A



For example, Figure 28A above illustrates that the switch 2816 (blue) receives a string of multiple pulses (modulated oscillating signal 2804) (green) and a bias signal 2806 (purple). The pulses (green) cause the *switch* (blue) to change between ON (closed state while the signal 2804 is being received) and OFF (open state when there is no signal being received).

> When *the switch 2816 is "open,"* the output 2822 of switch module 2802 is at substantially the same voltage level as bias signal 2806. . . . *When the modulated oscillating signal 2804 causes the switch 2816 to become "closed,"* the output 2822 of switch module 2802 becomes connected electrically to the second input 2810 of switch module 2802. . . . *When the modulated oscillating signal 2804 causes the switch 2816 to again become "open,"* the amplitude of the harmonically rich signal 2814 again becomes equal to the bias signal 2806. . . . the *modulated oscillating signal 2804* [] *causes the switch 2816 to open and close.*

'508 patent, 35:63-66; 36:2-19.

As such, the *switch* is the *only* component that is "gating" the bias signal "under the control" of pulses. Thus, the *switch* is the disclosed structure. *See Northrop*, 325 F.3d at 1352 ("Features that do not perform the recited function do not constitute corresponding structure and thus do not serve as claim limitations."); *Asyst Techs.*, 268 F.3d at 1371 ("The corresponding structure to a function set forth in a means-plus-function limitation *must actually perform the recited function*, not merely enable the pertinent structure to operate as intended . . . .").

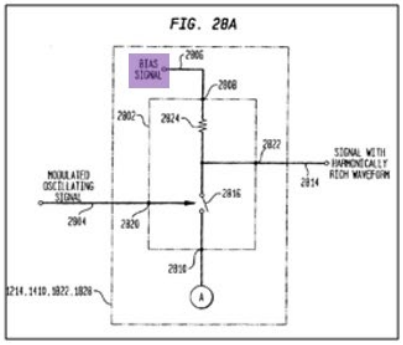
Intel, on the other hand, engages in a box-drawing exercise and attempts to expand the structure of the "gating means" to a larger structure that *includes* a switch – "switch module." But a switch "module" is *not* the actual structure that performs "gating" "under the control" of pulses. Only the *switch* within the switch module performs the claimed function.[21] For the foregoing reasons, the disclosed structure should only be a *switch*.

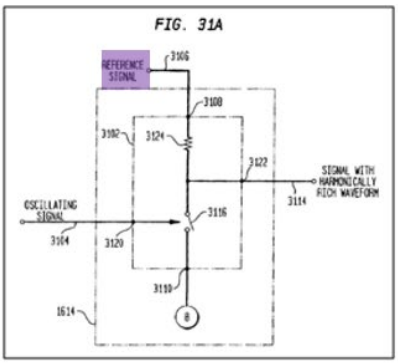
Dispute 2: Intel seeks to improperly exclude Figures 31A, 32A, 33A, 53, 54A, 55, 56 and 57A-C from the disclosed structure.

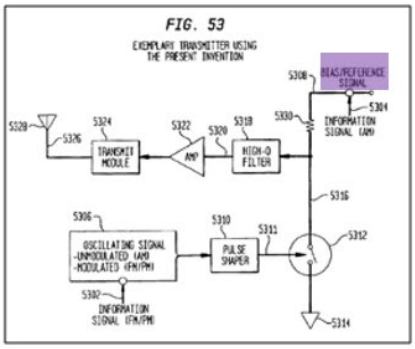
Claim 1 recites "gating a *bias signal*." A bias signal is a signal whose characteristics are modified in order to carry information. Intel agrees that Fig. 28A, 29A and 30A disclose "gating means"; these figures specifically recite a "bias signal."[22] *See* Figure 28A below left (purple).

[21] Intel focuses on the larger "switch module" because Intel seeks to capture the resistor 2824 in the definition of structure to support a non-infringement position. But a resistor does *not* perform the function of gating nor does a resistor open and close and, thus, a resistor is not "under the control" of anything, let alone pulses.

[22] Figures 54A, 57A, and 57B show a "bias signal" being sent to a switch. Thus, Figures 54A, 57A, and 57B should be included as claimed structures.







Intel, however, apparently seeks to exclude Figures 31A, 32A, 33A, 53, 54A, 55, 56 and 57A-C simply because, as shown above in purple (*e.g.,* Figure 31a and 53, middle and right above), these figures (1) refer to a bias signal as a "reference signal" or "bias/reference signal" or (2) a bias signal is combined with an information signal.[23]

But the specification states that "reference signal," "bias/reference signal," and "information signal" are types of "bias signals" or can be used as "bias signals." '508 patent, 59:4-6 ("In the *FM and PM modes*, *bias/reference signal* 5308 is . . . *often referred to simply as the bias signal*."); *id.* at 59:13-15 ("Typically, in the *AM mode*, this *bias/reference signal is referred to as the reference signal* to distinguish it from the bias signal used in the FM and PM modes.").[24] The specification states that the "information signal" may be used as the bias signal: "It is well known to those skilled in the relevant art(s) that the *information signal 5650 may be used as the bias/reference signal 5646* directly without being summed with a bias signal." *Id*. at 61:14-17. And even in an embodiment in which the bias signal is combined with an information signal, since the combined signal is being gated, the bias signal is gated. Thus, Figures 31A, 32A, 33A, 53, 54A, 55, 56 and 57A-C should be included as claimed structure.

[23] ParkerVision is not fully aware of the bases for Intel excluding these figures. As such, ParkerVision will respond to Intel's specific arguments in ParkerVision's Reply Brief.
[24] "FM" refers to frequency modulation, "PM" refers to phase modulation, and "AM" refers to amplitude modulation.

Though the Court will make its own determination regarding the meaning of "gating means," there is prior litigation history related to this term that ParkerVision would like to bring to the Court's attention. ParkerVision's construction of the structure of "gating means" adopts structure of the U.S. District Court for the Middle District of Florida (Orlando), Case No. 6:14-cv-687, which previously construed the structure of the "gating means" in a patent in the same family as the '508 patent. *See* Ex. 2 at 39. In reaching its construction, the Orlando court concluded that a skilled person can understand the meaning of "gating means" from Fig. 28A, 29A, 30A, 31A, 32A, 33A, 53, 54A, 55, 56, 57A-C. *Id*. at 39.[25]

For the foregoing reasons, Intel's construction should be rejected and ParkerVision's construction should be adopted.

D. "gating" (claim 1)

ParkerVision's Construction	Intel's Construction
"changing between the open and closed states of a switch, as dictated by an independent control input"	"opening and closing a device to selectively output a signal"

The parties agree that "gating" involves opening and closing a device. The parties disagree regarding (1) whether the device is a switch, (2) whether the device is "dictated by an independent control signal," (3) whether "gating" is "*changing* between the open and close states" or just the act of opening/closing, and (4) Intel's language "to selectively output a signal."

First, as discussed above in Section VI.C, gating is a function a *switch* performs. No other device performs the gating function.

Second, with regard to "as dictated by an independent control signal," this Court has already considered the issue in related 108 case when it construed a "switch" as "an electronic

[25] The Orlando court also included Figures 66-70. But these figures are not in the '508 patent.

device for opening and closing a circuit *as dictated by an independent control input*." Ex. 1 at 6. Indeed, claim 1 of the '508 patent recites "aperture generation means for generating *a string of multiple pulses*" and separate "gating means for gating a bias signal *under the control of said string of multiple pulses*." In other words, the "gating means" (switch) is "under control" of "pulses" that originate from an "aperture generation means," which the parties agree is a separate component from the switch. *See* Section VI.B above. As such, the switch is being controlled by an independent control signal (i.e., by a signal that originates external to the switch at the "aperture generation means").

Though the Court will make its own determination regarding the meaning of "gating," there is prior litigation history related to this term that ParkerVision would like to bring to the Court's attention. ParkerVision's construction of "gating" adopts the construction of the U.S. District Court for the Middle District of Florida (Orlando division) (Case No. 6:14-cv-687), which previously construed "gating" in the context of a patent in the same family as the '508 patent.[26] Ex. 2 at 38. In reaching its construction, the Orlando court looked to its construction of "switch/switch module" in determining that "gating" should include "as dictated by an independent control input." *Id*. at 34-35.

Third, gating is *not* merely the opening and closing a device. Rather, it is the process of *changing* between these two states i.e., between open and closed. Again, though the Court will make its own determination regarding the meaning of "gating," the Orlando court determined that gating was "*changing* between the open and closed states . . . ." *Id*. at 38.

Finally, Intel's language "to selectively output a signal" is wrong. Intel's language

[26] The Orlando court construed "gating" to mean: "changing between the open and closed states of a device that can take two states, open and closed, as dictated by an independent control input."

improperly sets forth a purpose of "gating." But the claim itself already recites a purpose of "gating" – "to generate a periodic signal having a plurality of harmonics." Moreover, Intel's language adds ambiguity because it is unclear what it means for a switch to "*selectively* output a signal." To the extent that "selectively" refers to outputting a signal only when the switch is ON (closed), such language can be readily understood based on context of the claim language.

For the foregoing reasons, Intel's construction should be rejected and ParkerVision's construction should be adopted.

E. "bias signal" (claim 1)

ParkerVision's Construction	Intel's Construction
"(1) a signal having a steady, predetermined level or (2) the modulating baseband signal"	"a signal having a fixed voltage or fixed current"

A bias signal can take different forms depending on the type of modulation technique being used – e.g., amplitude modulation (AM), phase modulation (PM) or frequency modulation (FM).

The specification discloses that a bias signal can be (1) a signal having a steady, predetermined level or (2) the modulating baseband signal. When FM and PM modulation techniques are used, the "bias signal" is a "non-varying signal" i.e., it has a steady, predetermined level: "In the FM and PM modes, bias/reference signal 5308 is preferably a non-varying signal, *often referred to simply as the* bias signal." '508 patent, 59:4-6. Moreover, the specification discloses that the bias signal can be the "modulating baseband signal." In particular, the specification states that an information signal can be used as the bias signal: "It is well known to those skilled in the relevant art(s) that the *information signal 5650 may be used as the bias/reference signal 5646* directly without being summed with a bias signal." *Id*. at 61:14-17. And the specification states an information signal (bias signal) which modulates a carrier signal

is a "modulating baseband signal": "When it is intended that the *information signal modulate a carrier signal*, it is also referred to as the '*modulating baseband signal*.'" *Id*. at 10:14-16. As such, ParkerVision's construction includes two types of signals.

Though the Court will make its own determination regarding the meaning of "bias signal," there is prior litigation history related to this term that ParkerVision would like to bring to the Court's attention. ParkerVision's constructions of "bias signal" adopts the constructions of the U.S. District Court for the Middle District of Florida (Orlando division) (Case No. 6:14-cv-687), which previously construed "bias signal" in the grandparent patent of the '508 patent.[27] *See* Ex. 2 at 50.

Intel's construction, on the other hand, is wrong because Intel seeks to *limit* "bias signal" to an *embodiment* of a signal with a "fixed voltage." The specification, however, states that the "bias signal" is "generally" a fixed voltage; the specification does *not* say the signal *must always* be a fixed voltage. *See, e.g.,* '508 patent, 34:34-37 ("A bias signal 2806 is gated as a result of the application of a modulated oscillating signal 2804, and a signal with a harmonically rich waveform 2814 is created. The *bias signal* 2806 is *generally* a *fixed voltage*."); *id.* at 35:17-19 ("A bias signal 2806 is applied to the first input 2808 of the switch module 2802. *Generally*, the bias signal 2806 is a *fixed voltage*, . . ."). As discussed above, however, a bias signal can also be the information signal (the modulating baseband signal).

For the foregoing reasons, Intel's construction should be rejected and ParkerVision's construction should be adopted.

F. "generating a string of multiple pulses from said string of pulses" (claim 1)

ParkerVision's Construction	Intel's Construction

[27] The Orlando court construed "bias signal" to mean: "(1) a signal having a steady, predetermined level; or (2) the modulating baseband signal." Ex. 2 at 50.

Plain and ordinary meaning	"generating a signal with multiple the number of pulses as said string of pulses"

Through its construction, Intel seeks to *re-write* the claim language to *exclude* an embodiment set forth in the specification.

Claim 1 of the '508 patent recites "aperture generation means coupled to said pulse shaping means for generating a string of multiple pulses from said string of pulses."

FIG. 78

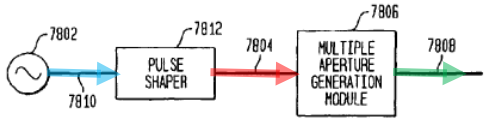


Figure 78 above illustrates the components set forth in claim 1 – "aperture generation means" is the multiple aperture generation module 7806; "pulse shaping means" is the pulse shaper 7812. Figure 78 illustrates how to create a control signal, which is sent to a switch to cause the switch to turn ON and OFF and, thus, gate a bias signal. '508 patent, 49:46-53. In particular, the local oscillator generates an oscillating signal 7810 (blue). *Id*. A pulse shaper 7812 receives the oscillating signal 7810 and outputs the claimed "string of pulses" 7804 (red). *Id*. The multiple aperture generation module 7806 receives the "string of pulses" and "generates a string of multiple pulses [green] from said string of pulses." *Id*. The "string of multiple pulses" is the control signal that is sent to the switch.

FIG. 80

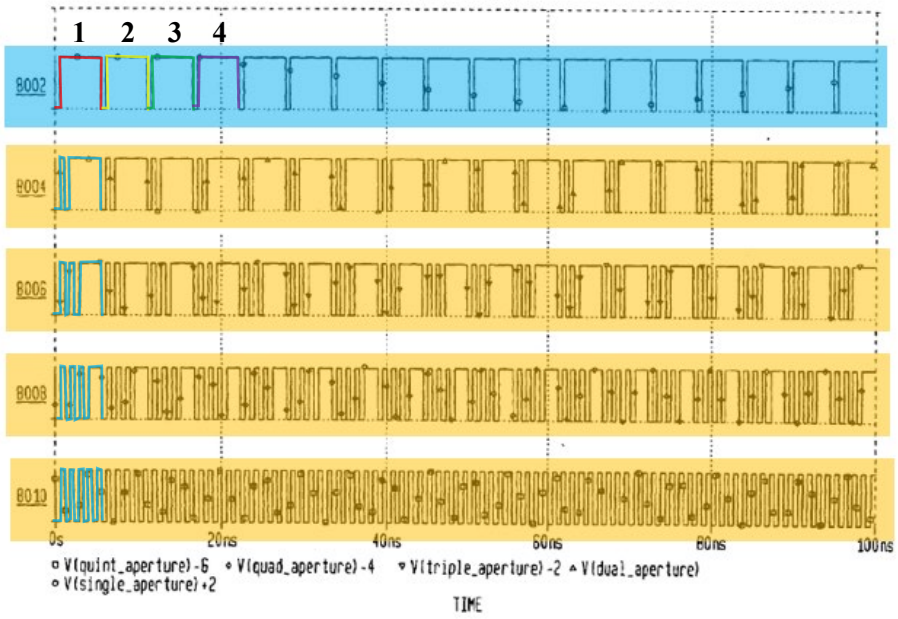


Figure 80 above illustrates the different types of pulse trains (each a "string of multiple pulses") that are outputted from the aperture generation module 7806. Specifically, the aperture generation module 7806 can output *either* pulse trains 8002, 8004, 8006, 8008 or 8010 (shown below highlighted in blue and orange). *Id*. at 50:23-36.

Pulse train 8002 (blue highlight) includes "a string of *multiple* pulses" as claimed – the first pulse (red line), the second pulse (yellow line), the third pulse (green line), the fourth pulse (purple line). Pulse train 8002 has *one* pulse for *each* pulse of the string of pulses from pulse shaper 7812. *Id*. at 50:6-12. As shown in Figure 80 above, pulse trains 8004, 8006, 8008 and 8010 (orange highlights) are different. As shown by the blue lines, for *each* pulse of the string of pulses from pulse shaper 7812: pulse train 8004 has *two* pulses, pulse train 8006 has *three* pulses, pulse train 8008 has *four* pulses, and pulse train 8010 has *five* pulses. *Id*.

But to preserve a potential non-infringement position, Intel seeks to exclude pulse train 8002. Thus, Intel has effectively *re-written* the language "multiple pulses" to be "multiple the number of pulses." Whereas pulse train 8002 has "multiple pulses" as claimed, pulse train 8002

does not have "multiple the number of pulses." Only pulse trains 8004, 8006, 8008 and 8010 have "multiple the number of pulses." But there is no basis for Intel to re-write the claims to exclude the embodiment of pulse train 8002.

For the foregoing reasons, Intel's construction should be rejected and the term should be given its plain and ordinary meaning.

VII. U.S. Patent No. 8,190,108 – Disputed claim constructions

A. "control signal" (claim 1)

ParkerVision's Construction	Intel's Construction
Plain and ordinary meaning	"an oscillating signal that controls the first switch with a frequency that is a sub-harmonic of and lower than the desired output frequency"

The words of this term are readily understandable to a jury. Claim 1 recites "a first switch configured to up-convert a signal based on a control signal." As such, a control signal is simply a signal that controls a switch and, thus, should be given its plain and ordinary meaning.

ParkerVision is not aware of the basis for Intel's construction and will respond to Intel's specific arguments in ParkerVision's Reply Brief.

Nevertheless, on its face, Intel's construction is wrong because it requires the "control signal" to "control[] the *first* switch." But a "control signal" is *not* specific to a "*first* switch." Looking at the use of "first switch" in claims 1 and 12, however, demonstrates that Intel's construction is wrong. In particular, claim 1 recites a first switch controlled by a control signal: "A frequency conversion module, comprising: a *first switch* configured to up-convert a signal *based on a control signal*." Claim 12, however, recites that a *third* switch, *not* the first switch, is controlled by a control signal: "the frequency conversion module comprises a *third switch* and is configured to *up-convert* the signal" "up-converting a signal *based on a control signal.*" As such, contrary to Intel's construction, the control signal is *not* always associated with the "first switch."

For the foregoing reasons, Intel's construction should be rejected and the term should be given its plain and ordinary meaning.

B. "third switch" (claim 1)

ParkerVision's Construction	Intel's Construction
Plain and ordinary meaning "switch" as construed by the Court in Case No. 6:20-cv-00108	"a switch controlling whether the antenna transmits said signal"

The term is straight-forward and does not require a construction other than "switch," which the Court has previously construed in related 108 case. *See* Ex. 1 at 6. No further construction is required.

Intel, however, attempts to assign a special meaning to "third switch" based on the use of third switch in claim 1. But looking at the use of "third switch" in claims 1 and 12 demonstrates that Intel's construction is wrong. In particular, claim 1 recites a first and third switch: "A frequency conversion module, comprising: a *first switch* configured to *up-convert* a signal . . . wherein said signal is transmitted by an *antenna* connected to a *third switch*." In claim 1, the first switch is involved in up-conversion and the third switch relates to an antenna. Claim 12 also recites a first and third switch, but their roles are *reversed* from claim 1: "the frequency conversion module comprises a *third switch* and is configured to *up-convert* the signal" and "wherein the signal is routed to an *antenna* via a *first switch*." In claim 12, the first switch relates to an antenna and the third switch is involved in up-conversion. Contrary to Intel's construction, this demonstrates that "third switch" is *not* always associated with the antenna.

Moreover, Intel's construction is wrong because it improperly injects *function* language into the claim. Claim 1, however, only requires that a third switch is connected to an antenna; claim 1 does not require a special purpose (controlling an antenna) of a third switch that Intel

recites in its construction.

For the foregoing reasons, Intel's construction should be rejected and the term should be given its plain and ordinary meaning with the term "switch" having the construction the Court provided in related 108 case. *See* Ex. 1 at 6.

C. "pulse shaper" (claim 6)

ParkerVision's Construction	Intel's Construction
"circuitry that generates a string of pulses"	"a circuit configured to enhance a desired harmonic by shaping an oscillating signal"

The concept of a pulse shaper is straight forward. A signal is sent to a pulse shaper which generates a string of pulses. ParkerVision's construction captures this concept. Indeed, generating a string of pulses is simply what a pulse shaper does as repeatedly set forth in the specification:

> A local oscillator 5206 generates an oscillating signal 5228 which is routed through a *pulse shaper 5208*. The *result is a string of pulses 5230*. '108 patent, 53:47-49
>
> Oscillating signal 5436 is *shaped by pulse shaper* 5438 *to produce a string of pulses* 5440. *Id*. at 54:59-60.
>
> Oscillation signal 5436 is *routed through pulse shaper 5438 to create a string of pulses* 5440 . . . . *Id*. at 55:12-13.
>
> The oscillating signal is *shaped by pulse shaper 5632 and a string of pulses 5634 is created*. *Id*. at 56:4-6.
>
> Accordingly, as is apparent from FIGS. 39B-39D, *pulse shaper 3900 receives a square wave and generates a string of pulses* . . . . *Id*. at 45:12-15.
>
> Accordingly, as is apparent from FIGs. 40B-40D, pulse shaper 4000 receives a square wave and generates a string of pulses . . . . *Id*. at 45:44-47.
>
> [T]he *pulse shaper is configured to generate a string of pulses* based on the oscillating signal. *Id*. at claims 8, 19.

Intel seeks to limit "pulse shaper" to a specific embodiment. ParkerVision, however, is not aware of the basis for Intel's construction and will respond to Intel's specific arguments in ParkerVision's Reply Brief.

For the foregoing reasons, Intel's construction should be rejected and ParkerVision's construction should adopted.

Dated: February 15, 2021

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